KONGU ENGINEERING COLLEGE, PERUNDURAI, ERODE – 638 052
(Autonomous)

M.E. DEGREE IN VLSI DESIGN (FULL-TIME)

CURRICULUM

(For the candidates admitted from academic year 2014 – 15 onwards)

SEMESTER – I

Course Code	Course Title	Hours/ Week			Credit	Maximum Marks		
		L	T	P		CA	ESE	Total
	THEORY							
14AMT15	Applied Mathematics for Electronic Engineers	3	1	0	4	40	60	100
14VLT11	Digital System for IC Design	3	1	0	4	40	60	100
14VLT12	VLSI Design Techniques	3	0	0	3	40	60	100
14VLT13	VLSI Signal Processing	3	1	0	4	40	60	100
14VLT14	Device Modeling	3	0	0	3	40	60	100
14VLT15	HDL for IC Design	3	1	0	4	40	60	100
	PRACTICAL							
14VLL11	VLSI Design Laboratory-I	0	0	3	1	100	0	100
				Total	**23**			

CA - Continuous Assessment, ESE – End Semester Examination

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M.E. DEGREE IN VLSI DESIGN (FULL-TIME)

CURRICULUM

(For the candidates admitted from academic year 2014 – 15 onwards)

SEMESTER – II

Course Code	Course Title	Hours/ Week			Credit	Maximum Marks		
		L	T	P		CA	ESE	Total
	THEORY							
14VLT21	Analog VLSI Design	3	0	0	3	40	60	100
14VLT22	Application Specific Integrated Circuits Design	3	0	0	3	40	60	100
14VLT23	Testing of VLSI Circuits	3	1	0	4	40	60	100
14VLT24	Digital Signal Processing Integrated Circuits	3	1	0	4	40	60	100
	Elective-I (Professional)	3	0	0	3	40	60	100
	Elective-II (Professional)	3	0	0	3	40	60	100
	PRACTICAL							
14VLL21	VLSI Design Laboratory-II	0	0	3	1	100	0	100
14VLL22	ASIC Design Laboratory	0	0	3	1	100	0	100
				Total	**22**			

CA - Continuous Assessment, ESE – End Semester Examination

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M.E. DEGREE IN VLSI DESIGN (FULL-TIME)

CURRICULUM

(For the candidates admitted from academic year 2014 – 15 onwards)

SEMESTER – III

Course Code	Course Title	Hours/ Week			Credit	Maximum Marks		
		L	T	P		CA	ESE	Total
	THEORY							
	Elective-III (Professional)	3	0	0	3	40	60	100
	Elective-IV (Professional)	3	0	0	3	40	60	100
	Elective-V (Open)	3	0	0	3	40	60	100
	PRACTICAL							
14VLP31	Project Work - Phase I	0	0	12	6	50	50	100
				Total	**15**			

CA - Continuous Assessment, ESE – End Semester Examination

SEMESTER – IV

Course Code	Course Title	Hours/ Week			Credit	Maximum Marks		
		L	T	P		CA	ESE	Total
	PRACTICAL							
14VLP41	Project Work – Phase II	0	0	24	12	100	100	200
				Total	**12**			

CA - Continuous Assessment, ESE – End Semester Examination

Total Credits: 72

KONGU ENGINEERING COLLEGE, PERUNDURAI, ERODE – 638 052
(Autonomous)

M.E. DEGREE IN VLSI DESIGN (PART TIME)
CURRICULUM
(For the candidates admitted from academic year 2014 – 15 onwards)

SEMESTER – I

Course Code	Course Title	Hours/ Week			Credit	Maximum Marks		
		L	T	P		CA	ESE	Total
	THEORY							
14AMT15	Applied Mathematics for Electronic Engineers	3	1	0	4	40	60	100
14VLT15	HDL for IC Design	3	1	0	4	40	60	100
14VLT12	VLSI Design Techniques	3	0	0	3	40	60	100
	PRACTICAL							
14VLL11	VLSI Design Laboratory-I	0	0	3	1	100	0	100
				Total	**12**			

CA - Continuous Assessment, ESE – End Semester Examination

SEMESTER – II

Course Code	Course Title	Hours/ Week			Credit	Maximum Marks		
		L	T	P		CA	ESE	Total
	THEORY							
14VLT21	Analog VLSI Design	3	0	0	3	40	60	100
14VLT22	Application Specific Integrated Circuits Design	3	0	0	3	40	60	100
14VLT23	Testing of VLSI Circuits	3	1	0	4	40	60	100
	PRACTICAL							
14VLL22	ASIC Design Laboratory	0	0	3	1	100	0	100
				Total	**11**			

CA - Continuous Assessment, ESE – End Semester Examination

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(Autonomous)

M.E. DEGREE IN VLSI DESIGN (PART TIME)

CURRICULUM

(For the candidates admitted from academic year 2014 – 15 onwards)

SEMESTER – III

Course Code	Course Title	Hours/ Week			Credit	Maximum Marks		
		L	T	P		CA	ESE	Total
	THEORY							
14VLT11	Digital System For IC Design	3	1	0	4	40	60	100
14VLT13	VLSI Signal Processing	3	1	0	4	40	60	100
14VLT14	Device Modeling	3	0	0	3	40	60	100
				Total	**11**			

CA - Continuous Assessment, ESE – End Semester Examination

SEMESTER – IV

Course Code	Course Title	Hours/ Week			Credit	Maximum Marks		
		L	T	P		CA	ESE	Total
	THEORY							
14VLT24	Digital Signal Processing Integrated Circuits	3	1	0	4	40	60	100
	Elective-I (Professional)	3	0	0	3	40	60	100
	Elective-II (Professional)	3	0	0	3	40	60	100
	PRACTICAL							
14VLL21	VLSI Design Laboratory-II	0	0	3	1	100	0	100
				Total	**11**			

CA - Continuous Assessment, ESE – End Semester Examination

KONGU ENGINEERING COLLEGE, PERUNDURAI, ERODE – 638 052
(Autonomous)

M.E. DEGREE IN VLSI DESIGN (PART TIME)

CURRICULUM

(For the candidates admitted from academic year 2014 – 15 onwards)

SEMESTER – V

Course Code	Course Title	Hours/ Week			Credit	Maximum Marks		
		L	T	P		CA	ESE	Total
	THEORY							
	Elective-III (Professional)	3	0	0	3	40	60	100
	Elective-IV (Professional)	3	0	0	3	40	60	100
	Elective-V (Open)	3	0	0	3	40	60	100
	PRACTICAL							
14VLP31	Project Work - Phase I	0	0	12	6	50	50	100
				Total	**15**			

CA - Continuous Assessment, ESE – End Semester Examination

SEMESTER – VI

Course Code	Course Title	Hours/ Week			Credit	Maximum Marks		
		L	T	P		CA	ESE	Total
	PRACTICAL							
14VLP41	Project Work - Phase II	0	0	24	12	100	100	200
				Total	**12**			

CA - Continuous Assessment, ESE – End Semester Examination

Total Credits: 72

LIST OF ELECTIVES					
Course Code	**Course Title**	**Hours/Week**			**Credit**
		L	**P**	**T**	
14VLE01	Low Power Design of VLSI Circuits	3	0	0	3
14VLE02	VLSI Technology	3	0	0	3
14VLE03	Computer Aided Design of VLSI Circuits	3	0	0	3
14VLE04	Intellectual Property based VLSI Design	3	0	0	3
14VLE05	Analysis and Design of Digital Integrated Circuits	3	0	0	3
14VLE06	Electronic Design Automation Tools	3	0	0	3
14VLE07	Optimization Techniques for VLSI Circuits	3	0	0	3
14VLE08	Reconfigurable Architectures for VLSI	3	0	0	3
14VLE09	RF VLSI Design	3	0	0	3
14VLE10	Nano Electronics *	3	0	0	3
14MME03	MEMS Design	3	0	0	3
14COE16	Electromagnetic Interference and Compatibility	3	0	0	3
14VLE11	Design of Semiconductor Memories	3	0	0	3
14VLE12	DSP Processor Architecture and Programming	3	0	0	3
14VLE13	Genetic Algorithms *	3	0	0	3
14VLE14	Submicron VLSI Design	3	0	0	3
14VLE15	VLSI for Wireless Communication	3	0	0	3
14VLE16	Hardware Software Co-Design	3	0	0	3
14COE05	Digital Image Processing and Multi Resolution Analysis	3	0	0	3
14COT11	Statistical Signal Processing	3	1	0	4

*- Open Elective

14AMT15 APPLIED MATHEMATICS FOR ELECTRONIC ENGINEERS

(Common to VLSI Design & Embedded Systems)

3 1 0 4

UNIT – I **9**

Vector Spaces: Definition – Subspaces – Span – Linear dependence and independence – Basis and dimension – Row space, Column space and Null Space – Rank and nullity.

UNIT – II **9**

Inner Product Spaces: Inner products – Angle and Orthogonality in inner product spaces – Orthonormal Bases – Gram-Schmidt Process – QR-Decomposition – Orthogonal Projection – Least square technique – Orthogonal matrices.

UNIT – III **9**

Graph Theory: Introduction of graphs – Isomorphism – Subgraphs – Walks, paths and circuits – Connected graphs – Eulerian Graphs – Hamiltonian Paths and circuits – Digraph – Some types of digraphs – Connectedness – Adjacency matrix and incidence matrix of graphs – Shortest path algorithms – Dijkstra's algorithm – Warshall's algorithm – Trees – Properties of trees – Spanning trees – Minimal spanning trees – Prim's Algorithm – Kruskal's algorithm.

UNIT – IV **9**

Stochastic Process: Definition – Classification of Stochastic Processes – Markov Chain -Transition Probability Matrices – Chapman Kolmogorov Equations - Classification of States – Continuous Time Markov Chains – Poisson Process - Birth and Death Processes.

UNIT – V **9**

Queuing Theory: Markovian queues – Single and Multi-server Models – Little's formula – Machine Interference Model - Non- Markovian Queues – Pollaczek Khintchine Formula.

Lecture: 45, Tutorial: 15, TOTAL: 60

REFERENCE BOOKS:

1. Howard Anton, Chris Rorres, "Elementary Linear Algebra" John Wiley & Sons, 2010.
2. David C Lay, "Linear Algebra and Its Applications", Pearson Education, 2009.
3. Richard Bronson, Gabriel B.Costa, "Linear Algebra", Academic Press, Second Edition, 2007.
4. Narsing Deo, "Graph Theory with Applications to Engineering and Computer science", Prentice Hall of India limited, 2005.
5. Roy D.Yates and David J Goodman, "Probability and Stochastic Processes – A friendly Introduction for Electrical and Computer Engineers", John Wiley & Sons, 2005.
6. Donald Gross and Carl M. Harris, "Fundamentals of Queuing theory", 2nd edition, John Wiley and Sons, New York (1985).

Course Outcomes:

On the completion of the course the students will be able to

- handle problems in linear algebra
- adopt graph theoretical concepts in electronics
- process information using random process

14VLT11 DIGITAL SYSTEM FOR IC DESIGN

3 1 0 4

Pre-requisites: Digital Electronics

UNIT – I **9**

Synchronous Sequential Circuit Design: Analysis of Clocked Synchronous Sequential Networks (CSSN)- Modeling of CSSN – State table Reduction- Stable Assignment – Complete Design of CSSN – Design of Iterative Circuits.

UNIT – II **9**

Algorithmic State Machine (ASM): ASM-ASM Chart – Synchronous Sequential Network Design Using ASM Charts- State Assignment- ASM Tables-ASM Realization- Asynchronous Inputs.

UNIT – III **9**

Asynchronous Circuit Design: Analysis of Asynchronous Sequential Circuit (ASC) – Flow Table Reduction – Races in ASC – State Assignment – Problem and the Transition Table – Design of ASC – Static and Dynamic Hazards – Essential Hazards

UNIT – IV **9**

Programming Logic Arrays: PLA minimization – Essential Prime Cube theorem- PLA folding- foldable compatibility matrix- The Compact Algorithm. Practical PLA's –Data Synchronizers – Designing Vending Machine Controller – Mixed Operating Mode Asynchronous Circuits

UNIT – V **9**

Programmable Devices: Programmable Logic Devices – Designing a Synchronous Sequential Circuit using a PAL – Realization of State machine using PLD –Complex Programmable Logic Devices (CPLDs) – FPGA – Xilinx FPGA – Xilinx 3000 - Xilinx 4000.

Lecture: 45, Tutorial: 15, TOTAL: 60

REFERENCE BOOKS::

1. Givone Donald G., "Digital Principles and Design", Tata McGraw-Hill, New Delhi, 2002
2. Biswas Nripendra N, "Logic Design Theory", Prentice Hall of India, New Delhi, 2001
3. Yarbrough, John M., "Digital Logic Applications and Design", Thomson Learning, Singapore, 2001.
4. Roth Charles H., "Fundamentals of Logic Design", Thomson Learning, Singapore, 2005
5. Ming-Bo Lin, "Digital System Design and Practices: Using Verilog HDL and FPGAs", Wiley Publisher, New York, 2008.

Course Outcomes:

On completion of the course the students will be able to

- analyze and design synchronous and asynchronous circuits
- design synchronous circuits using PLDs
- analyze different architectures of Xilinx FPGAs for implementation

14VLT12 VLSI DESIGN TECHNIQUES

3 0 0 3

Pre-requisites: VLSI Design

UNIT – I **9**

MOS Transistor Theory: NMOS and PMOS transistors, CMOS logic, MOS transistor theory – Introduction, Enhancement mode transistor action, Ideal I-V characteristics, DC transfer characteristics, Threshold voltage-Body effect- Design equations- Second order effects. MOS models and small signal AC characteristics.

UNIT – II **9**

CMOS Technology and Design Rule: CMOS fabrication and Layout, CMOS technologies: P -Well process, N -Well process, twin –tub process, SOI - MOS layer stick diagram and Layout diagram, Layout design rules, Latch up in CMOS circuits, CMOS process enhancements, Technology – related CAD issues, Fabrication and packaging.

UNIT – III **9**

Circuit Characterization and Performance Estimation: Resistance estimation, Capacitance estimation, Inductance, switching characteristics, transistor sizing, power dissipation and design margining-Charge sharing-Scaling

UNIT – IV **9**

Combinational and Sequential Circuit Design: Transmission gates, combinational Circuit Design – static CMOS, Ratioed Circuits, Cascode Voltage Switch logic, Dynamic Circuits, Pass transistor circuits, Differential circuits, sense amplifier circuits, BICMOS circuits, comparison. Sequential Circuit Design – Latches and flipflops.

UNIT – V **9**

VLSI System Components Circuits and System Level Physical Design: Multiplexers, Decoders, comparators, priority encoders, Shift registers. Arithmetic circuits – Ripple carry adders, Carry look ahead adders, High-speed adders, Multipliers. Physical design – Delay modeling ,power distribution. Clock distribution

TOTAL: 45

REFERENCE BOOKS::

1. Neil H.E. Weste and Kamran Eshraghian, Principles of CMOS VLSI Design, Pearson Education ASIA, Third edition, 2007.
2. Pucknell, “Basic VLSI Design”, Prentice Hall of India Publication, 1995.
3. Eugene D.Fabricius, Introduction to VLSI Design McGraw Hill International Editions, 1990
4. John P.Uyemura “Introduction to VLSI Circuits and Systems”, John Wiley & Sons, Inc., 2002.
5. Wayne Wolf “Modern VLSI Design System on chip. Pearson Education, 2002.

Course Outcomes:

On completion of the course the students will be able to

- fabricate and design MOS transistor
- develop combinational and sequential circuits using MOS transistor

14VLT13 VLSI SIGNAL PROCESSING

(Common to VLSI Design & Applied Electronics)

3 1 0 4

Pre-requisites: Digital Signal Processing

UNIT – I **9**

Introduction to DSP Systems: Introduction To DSP Systems -Typical DSP algorithms; Iteration Bound – data flow graph representations, loop bound and iteration bound, Algorithms For Computing Iteration Bound, Iteration Bound of Multirate Data Flow Graphs. Pipelining and parallel processing – Pipelining of FIR digital filters, parallel processing, pipelining and parallel processing for low power

UNIT – II **9**

Retiming and Unfolding: Retiming - definitions and properties Retiming techniques; Solving systems of inequalities, Retiming Techniques. Unfolding – an algorithm for Unfolding, properties of unfolding, Critical path Unfolding and Retiming applications of Unfolding- sample period reduction and parallel processing application

UNIT – III **9**

Folding: Folding – Folding transformation – Register minimizing techniques –Register minimization in folded architectures-Folding of Multirate systems.

Fast Convolution: Fast convolution – Cook-Toom algorithm, modified Cook-Took algorithm – Wino grad Algorithm, Modified Wino grad Algorithm -Design of Fast Convolution algorithm by inspection

UNIT – IV **9**

Algorithmic strength reduction: Algorithmic strength reduction in Filters-Parallel FIR Filters, DCT and Inverse DCT, Parallel architectures for rank order Filters.

UNIT – V **9**

Pipelined and Parallel Recursive filters Adaptive Filters:– Inefficient/efficient single channel interleaving, Look- Ahead pipelining in first- order IIR filters, Look-Ahead pipelining with power-of-two decomposition parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters, pipelined adaptive digital filters-relaxed look-ahead, pipelined LMS adaptive filter.

Lecture: 45, Tutorial: 15, TOTAL: 60

REFERENCE BOOKS::

1. Parhi, Keshab K., "VLSI Digital Signal Processing Systems, Design and Implementation", John Wiley, Inter Science, New York, 1999.
2. Isamail, Mohammed and Fiez, Terri, "Analog VLSI Signal and Information Processing", McGraw-Hill, New York, 1994**.**
3. www.pdf-search-engine.com/vlsi-signal-processing-pdf.html
4. Magdy A. Bayoumi, Magdy A. Bayoumi, E. Swartzlander, "VLSI Signal Processing Technology", Kluwer Academic Publishers.October 1994
5. Ray Liu K J, "High Performance VLSI Signal Processing, Innovative architectures and Algorithms",IEEE Press,1998

Course Outcomes:

On completion of the course the students will be able to

- design filters using the concept of retiming, folding and unfolding techniques
- analyse and design pipelined and parallel recursive adaptive filters

14VLT14 DEVICE MODELING

(Common to VLSI Design & Applied Electronics)

3 0 0 3

Pre-requisites: Electron Devices

UNIT – I **9**

Semiconductor Physics and Modeling of Passive Devices: Carrier Concentration- Transport Equation- Mobility and Resistivity- Carrier Diffusion- Carrier Generation and Recombination-Continuity equation- Modeling of Resistors-Modeling of Capacitors-Modeling of Inductors.

UNIT – II **9**

Diode and Bipolar Device Modeling : Abrupt and linear graded PN junction- Ideal diode current equation- Static, Small signal and Large signal models of PN junction Diode-SPICE model for a Diode- Temperature and Area effects on Diode Model Parameters Transistor Action-Terminal currents -Switching- Static, Small signal and Large signal Eber-Moll models of BJT-Temperature and area effects

UNIT – III **9**

MOSFET Modeling: MOS Transistor – NMOS- PMOS – MOS Device equations - Threshold Voltage – Second order effects - Temperature Short Channel andNarrow Width Effect- Models for MOSFET.

UNIT – IV **9**

Noise Models and BSIM4 MOSFET Model: Noise Sources in MOSFET-Flicker Noise Modeling-Thermal Noise Modeling- BSIM4 MOSFET Model-Gate Dielectric Model-Enhanced Models for Effective DC and AC Channel Length and width-Threshold Voltage Model-I-V Model.

UNIT – V **9**

Other MOSFET Models: EKV Model-Model Features-Long Channel Drain Current Model-Modeling Second order Effects of Drain Current-Effect of Charge Sharing-Modeling of Charge storage Effects-Non-quasi static Modeling-Noise Models-Temperature Effects-MOS Model 9-MOSAI Model

TOTAL: 45

REFERENCE BOOKS::

1. Massobrio Giuseppe and Antognetti Paolo, “Semiconductor Device Modeling with SPICE”, Second Edition, McGraw-Hill Inc, New York, 1993
2. Sze S. M., “Semiconductor Devices-Physics and Technology”, 2nd Edition, John Wiley and Sons, New York, 2002.
3. Trond Ytterdal,Yuhua Cheng and Tor A.Fjeldly,,”Device Modeling for Analog and RF CMOS Circuit Design”John Wiley &Sons Ltd ,2003.
4. M.S. Tyagi, “Intorduction to Semiconductor Materials and Devices”, John Wiley, New York, 2003
5. Ben,G.Streetman, “Solid State Circuits”, 5th Edition, Prentice Hall of India, New Delhi, 2005.
6. De Graaf H.C and Klaasen F M.- “Compact Transistor Modeling for Circuit Design”, SpringerVerlag, New York,1990.

Course Outcomes:

On completion of the course the students will be able to

- analyze different properties and characteristics of semiconductor devices for developing applications
- model and simulate diodes and transistors

14VLT15 HDL FOR IC DESIGN

3 1 0 4

Pre-requisites: Digital Electronics

UNIT – I **9**

Introduction to VHDL: VHDL Description of combinational Network-Modeling FF using VHDL process-VHDL model for a multiplexer-Compilation and Simulation of VHDL Code-Modeling a Sequential Machine-Variable, Signals and Constants-Arrays-VHDL Operators-VHDL functions – VHDL Procedures-Packages and Libraries.

UNIT – II **9**

Design using VHDL: Design of a Serial Adder with accumulator, State Graph for a control network-Design of Binary Multiplier-Multiplication of signed binary number-Design of a binary divider-Binary decoder-Binary encoder-Multiplexer-Demultiplexer

UNIT – III **9**

Modeling Verilog HDL: Overview of digital design using Verilog HDL-Hierarchical Modeling concepts-Basic Concepts-Gate level Modeling-Dataflow Modeling-Behaviour Modeling-Tasks and Functions-Switch level modeling.

UNIT – IV **9**

Logic Synthesis using verilog HDL: Verilog HDL Synthesis-Synthesis Design Flow-Verification of the gate level net list-Modeling for logic synthesis-Example of sequential circuit synthesis

UNIT – V **9**

System Verilog: Introduction- Design Hierarchy- Data types- Operators and language constructs. Functional coverage- assertion- Interfaces and test bench structures.

Lecture: 45, Tutorial: 15, TOTAL: 60

REFERENCE BOOKS::

1. Roth C.H., "Digital System Design using VHDL", Thomson Learning, Singapore, 2001.
2. Navabi, "VHDL Analysis and Modeling of Digital Systems", McGraw-Hill, New York
3. Stephen Brown and Zvonko Vranesic, "Fundamentals of Digital Logic with VHDL Design", Second Edition, McGraw-Hill, New York, 2005
4. Samir Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", Pearson Education, New Delhi, 2003.
5. Stuart Sutherland, Simon Davidmann, and Peter Flake, "System Verilog for Design: "A Guide to Using SystemVerilog for Hardware Design and Modeling", 2nd Edition, Springer, 2010
6. Janick Bergeron, Eduard Cerny, Alan Hunter, Andy Nightingale "Verification Methodology Manual for SystemVerilog", Springer, 2005
7. Chris Spear SystemVerilog for Verification: "A Guide to Learning the Testbench Language Features", 3rd Edition, Springer, 2012

Course Outcomes:

On completion of the course the students will be able to

- program and simulate digital circuits using HDL
- develop various RTL level System

14VLL11 VLSI DESIGN LABORATORY-I

0 0 3 1

LIST OF EXPERIMENTS:
USING VHDL

1. Modeling of Sequential Digital Systems
2. Testbenches
3. State Machine Design
4. Memory Design
5. Design and implementation of ALU, MAC using FPGA
6. Design and implementation of different adders using FPGA
7. Design and implementation of Real time clock using FPGA
8. Design and implementation of 4 x 4 matrix keypad using FPGA
9. Design and implementation of UART using FPGA

SPICE MODELING (Microwind)

1. Simulation of NMOS circuits
2. Simulation of CMOS Circuits –Inverter, AND, OR
3. Simulation of CMOS Circuits –Half adder, full adder

TOTAL: 45

REFERENCES / MANUALS / SOFTWARE:

- Model Sim
- Xilinx
- Microwind

Course Outcomes:

On completion of the course the students will be able to

- implement various digital circuits in FPGA using VHDL
- design transistor level architecture for digital circuits

14VLT21 ANALOG VLSI DESIGN

3 0 0 3

Pre-requisites: VLSI Design Techniques

UNIT – I **9**

Basic CMOS Circuits: Mixed-Signal VLSI Chips-Basic CMOS Circuits-Basic Gain Stage-Gain Boosting Techniques-Super MOS Transistor- Primitive Analog Cells-Linear Voltage-Current Converters-MOS Multipliers and Resistors-CMOS, Bipolar and Low-Voltage BiCMOS Op-Amp Design-Instrumentation Amplifier Design-Low Voltage Filters.

UNIT – II **9**

Basic BiCMOS Circuits: Continuous-Time Signal Processing-Sampled-Data Signal Processing-Switched-Current Data Converters-Practical Considerations in SI Circuits Biologically-Inspired Neural Networks – Floating – Gate, Low-Power Neural Networks-CMOS Technology and Models-Design Methodology-Networks-Contrast Sensitive Silicon Retina.

UNIT – III **9**

Sampled-Data Analog Circuits : First-order and Second SC Circuits-Bilinear Transformation – Cascade Design-Switched-Capacitor Ladder Filter-Synthesis of Switched-Current Filter- Nyquist rate A/D Converters-Modulators for Over sampled A/D Conversion-First and Second Order and Multibit Sigma-Delta Modulators-Interpolative Modulators –Cascaded Architecture-Decimation Filters-mechanical, Thermal, Humidity and Magnetic Sensors-Sensor Interfaces.

UNIT – IV **9**

Design For Testability And Analog VLSI Interconnects : Fault modeling and Simulation – Testability-Analysis Technique-Ad Hoc Methods and General Guidelines-Scan Techniques-Boundary Scan-Built-in Self Test-Analog Test Buses-Design for Electron –Beam Testability-Physics of Interconnects in VLSI-Scaling of Interconnects-A Model for Estimating Wiring Density-A Configurable Architecture for Prototyping Analog Circuits

UNIT – V **9**

Statistical Modeling And Analog And Mixed Analog-Digital Layout : Review of Statistical Concepts – Statistical Device Modeling- Statistical Circuit Simulation-Automation Analog Circuit Design-automatic Analog Layout-CMOS Transistor Layout-Resistor Layout-Capacitor Layout-Analog Cell Layout-Mixed Analog –Digital Layout.

TOTAL: 45

REFERENCE BOOKS::

1. Ismail, Mohammed., Fiez, Terri., "Analog VLSI Signal and Information Processing", McGraw-Hill, New York, 1994
2. Haskard, Malcom R., May, Lan C., "Analog VLSI Design – NMOS and CMOS", Prentice Hall, New Jersey, 1998.
3. Geiger, Randall L, and Allen, Phillip E., Strader, Noel K., "VLSI Design Techniques for Analog and Digital Circuits", McGraw-Hill, New York, 1990.
4. France, Jose E., and Tsividis, Yannis., "Design of Analog Digital VLSI Circuits for Telecommunication and signal Processing", Prentice Hall, New Jersey, 1994.

Course Outcomes:

On completion of the course the students will be able to

- design CMOS and BiCMOS circuits
- model, simulate and test CMOS and BiCMOS circuits

14VLT22 APPLICATION SPECIFIC INTEGRATED CIRCUITS DESIGN

3 0 0 3

Pre-requisites: VLSI Design

UNIT – I **9**

Introduction to ASICs, CMOS Logic and ASIC Library Design: Types of ASICs - Design flow - CMOS transistors - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort.

UNIT – II **9**

Programmable ASICs, Programmable ASIC Logic Cells And Programmable ASIC I/O Cells : Anti fuse - static RAM - EPROM and EEPROM technology - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

UNIT – III **9**

Programmable ASIC Interconnect: Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX9000 - Altera FLEX –Design systems - Half gate ASIC –Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation.

UNIT – IV **9**

Architecture, synthesis and Physical Design : Architecture and configuration of Spartan / Cyclone and Virtex / Stratix FPGAs – Micro-Blaze / NIOS based embedded systems – Signal probing techniques Logic synthesis - ASIC floor planning- placement and routing – power and clocking strategies.

UNIT – V **9**

Optimization Algorithms: Planar subset problem(PSP) -single layer global routing single layer detailed routing wire length and bend minimization technique -over the cell(OTC) Routing-multichip modules(MCM)-Programmable logic arrays-Transistor chaining-Weinberger Arrays-Gate Matrix Layout-1D compaction-2D compaction

TOTAL: 45

REFERENCE BOOKS::

1. M.J.S.Smith, " Application - Specific Integrated Circuits", Pearson,2003
2. Steve Kilts, “Advanced FPGA Design,” Wiley Inter-Science
3. Roger Woods, John McAllister, Dr. Ying Yi, Gaye Lightbod, “FPGA-based Implementation of Signal Processing Systems”, Wiley, 2008
4. Mohammed Ismail and Terri Fiez, "Analog VLSI Signal and Information Processing ", Mc Graw Hill, 1994.
5. Douglas J. Smith, HDL Chip Design, Madison, AL, USA: Doone Publications, 1996.
6. Jose E. France, Yannis Tsividis, "Design of Analog - Digital VLSI Circuits for Telecommunication

Course Outcomes:

On completion of the course the students will be able to

- design ASIC logic cells, I/O cells, interconnect and architecture
- analyze high performance algorithms for ASIC design

14VLT23 TESTING OF VLSI CIRCUITS

3 1 0 4

Pre-requisites: Digital Circuits

UNIT – I **9**

Fault Modeling and Simulation Importance of Testing-Testing during the VLSI Lifecycle- Fault models- Levels of abstraction in VLSI testing-Simulation models- Logic Simulation-Fault Simulation

UNIT – II **9**

Design for Testability: Testability analysis –DFT Basics- Scan Cell Designs- Scan Architectures-Scan Design Rules- Scan Design Flow- RTL Design for Testability.

UNIT–III **9**

Test Generation: Random Test Generation- Designing a Stuck-at ATPG for Combinational Circuits-Designing a Sequential ATPG- Untestable Fault Identification- Designing Simulation based ATPG-Hybrid Deterministic and Simulation based ATPG- ATPG for Non-Stuck at Faults

UNIT– IV **9**

Built In Self Test: BIST Design rules- Test Pattern generation- Output Response Analysis- Logic BIST Architecture- Fault Coverage Enhancement- BIST Timing Control- Logic BIST System Design

UNIT – V **9**

Logic Diagnosis and Memory Testing: Combinational Logic Diagnosis- Scan Chain Diagnosis-Logic BIST Diagnosis- RAM functional Fault Models and Test Algorithms- RAM Fault Simulation and Test Algorithm Generation

Lecture: 45, Tutorial: 15, TOTAL: 60

REFERENCE BOOKS::

1. Laung – Terng wang, Cheng – wen wu, Xidogingwen, "VLSI Testing Principles and Architectures: Design for Testability", Morgan Kaufmann Publisher, 2006.
2. Abramovici, M., Breuer, M.A and Friedman, A.D., "Digital Systems and Testable Design", Jaico Publishing House, 2002.
3. Bushnell, M.L and. Agrawal, V.D., "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwar Academic Publishers, 2002.
4. Nilcolici Nicoda, Al- HAshmini, "Power constrained Testing of VLSI Circuits", Kluwer Academic Publishers,2003.
5. Laung – Terng wang,Charles E.Stroud and Nur A.Touba., "System on Chip Test Architectures: Nano meter design Design for Testability", Morgan Kaufmann Publisher, 2007.

Course Outcomes:

On completion of the course the students will be able to

- design DFT for VLSI circuits
- apply principles and algorithms for ATPG tools

14VLT24 DIGITAL SIGNAL PROCESSING INTEGRATED CIRCUITS

3 1 0 4

Pre-requisites: Digital Signal Processing

UNIT – I **9**

Scaling,Round off Noise: Standard digital signal processors, Application specific IC's for DSP, DSP systems, DSP system design,; Scaling and Round off Noise- State variable Description of digital filters, Scaling and round off noise computation, Round off noise in pipelined IIR filters, Round off noise computation using State Variable description..

UNIT – II **9**

Lattice Structure: Introduction, Schur algorithm, Digital basic Lattice Filters, Derivation of One-Multiplier Lattice Filter, Derivation of Normalized Lattice filter, Derivation of Scaled-Normalized Lattice Filter, Round off Noise Calculation in Lattice filters, Pipelining of Lattice IIR Digital Filters, Design Examples of Pipelined Lattice Filters, Low-Power CMOS Lattice IIR Filters

UNIT – III **9**

Redundant Arithmetic Number system representations, Redundant Arithmetic-Carry-Free Radix-2 Addition And Subtraction, Hybrid Radix-4 Addition, Radix-2 Hybrid Redundant Multiplication Architectures, Data Format Conversion, Redundant to Non redundant Converter, Numerical Strength Reduction-Introduction, Sub expression Elimination, Multiple Constant Multiplication, Sub expression Sharing in Digital Filters, Additive and Multiplicative Number Splitting.

UNIT – IV **9**

Bit-Level Arithmetic Architectures and Accumulator: Introduction, Parallel Multipliers, Interleaved Floor-Plan and Bit-Plane-Based Digital Filters, Bit-Serial Multipliers, Bit-Serial Filter Design and Implementation, Canonic Signed Digit Arithmetic, Distributed Arithmetic-Problems, Bit – Parallel and Bit-Serial Arithmetic. Basic Shift accumulator, Improved Shift accumulator.

UNIT – V **9**

Pipelining Concepts: Pipelining Concepts-Introduction, Synchronous Pipelining and Clocking Styles, Clock Skew and Clock Distribution in Bit-Level Pipelined VLSI Designs, Wave Pipelining, Constraint Space Diagram and Degree of Wave Pipelining, Implementation of Wave-Pipelined Systems, Asynchrounous Pipelining, Signal Transition Graphs, Use of STG to Design Interconnection Circuits, Implementation of Computational Units, Problems. Layout of VLSI Circuits, DCT Processor as case studies

Lecture: 45, Tutorial: 15, TOTAL: 60

REFERENCE BOOKS::

1. Parhi Keshab K.., " VLSI Digital Signal Processing Systems Design and Implementation" A Wiley-Interscience Publication, John Wiley & Sons,INC,1999.
2. Wanhammer, Lars., **"**DSP Integrated Circuits**"**, Academic press, New York, 1999.
3. Oppenheim, A.V and Schafer, Ronald W. "Discrete-Time Signal Processing", Pearson Education, 2000
4. Ifeachor, Emmanuel C. and Jervis, Barrie W., **"**Digital Signal Processing – A Practical Approach**",** 2nd Edition, Pearson Education Asia, 2001.
5. Perelroyzen E., "Digital Integrated circuits: Design- for- Test using Simulink and State flow", CRC press, 2006.

Course Outcomes:

On completion of the course the students will be able to

- implement the DSP concepts in VLSI architecture
- analyze and design various redundant and bit-level architectures

14VLL21 VLSI DESIGN LABORATORY-II

0 0 3 1

LIST OF EXPERIMENTS:

USING VERILOG

1. Modeling of Sequential Digital Systems
2. Test benches
3. State Machine Design
4. FIFO
5. Design and implementation of pipelined array multiplier using FPGA
6. Design and implementation of Traffic light controller using FPGA
7. Design and implementation of rolling display using FPGA
8. Design and implementation of stepper motor interface using FPGA
9. Implementation of various DSP algorithms

USING MICROWIND

1. Logic design using pass transistor and transmission gates
2. Multiplexer
3. Flipflops

TOTAL: 45

REFERENCES / MANUALS / SOFTWARE:

- Model Sim
- Xilinx
- Microwind

Course Outcomes:

On completion of the course the students will be able to

- implement various combinational and sequential circuits in FPGA using VHDL
- design transistor level architecture for combinational and sequential circuits

14VLL22 ASIC DESIGN LABORATORY

0 0 3 1

LIST OF EXPERIMENTS:
USING VERILOG

1. Static Timing analyses procedures and constraints. Critical path considerations
2. Scan chain insertion, Floor Planning, Routing and Placement procedures
3. Power Planning, Layout generation, LVS and Back annotation, Total power estimate. Analog Circuit simulation
4. Simulation of logic gates, current mirrors, Current Sources, Differential Amplifier in Spice
5. Layout generation, LVS, Back annotation

TOTAL: 45

REFERENCES / MANUALS / SOFTWARE:

- Synopsys – VCS, Design Vision, ICC, Custom Design, HSpice

Course Outcomes:

On completion of the course the students will be able to

- design analog and digital ASIC.
- measure and optimize various parameters

14VLE01 LOW POWER DESIGN OF VLSI CIRCUITS

(Common to VLSI Design & Applied Electronics)

3 0 0 3

Pre-requisites: VLSI Design Techniques

UNIT – I **9**

Power dissipation in CMOS: Hierarchy of limits of power – Sources of power consumption – Physics of power dissipation in CMOS FET devices – Long Channel and Submicron Effect-Basic principle of low power design.

UNIT – II **9**

Power optimization : Logic level power optimization – Circuit level low power design – circuit techniques for reducing power consumption in adders and multipliers.

UNIT – III **9**

Design of Low Power CMOS circuits : Computer arithmetic techniques for low power system – reducing power consumption in memories – low power clock, Inter connect and layout design – Advanced techniques –Special techniques.

UNIT – IV **9**

Power estimation: Power Estimation techniques – logic power estimation – Simulation power analysis –Probabilistic power analysis.

UNIT – V **9**

Synthesis and software design for low power : Synthesis for low power – Behavioral level transform – software design for low power.

TOTAL: 45

REFERENCE BOOKS::

1. Kaushik Roy and S.C.Prasad, “Low power CMOS VLSI circuit design”, Wiley, 2000.
2. Dimitrios Soudris, Chirstian Pignet, Costas Goutis, “Designing CMOS Circuits for Low Power”, Kluwer, 2002.
3. J.B.Kulo and J.H Lou, “Low voltage CMOS VLSI Circuits”, Wiley 1999
4. A.P.Chandrasekaran and R.W.Broadersen, “Low power digital CMOS design”, Kluwer,1995
5. Gary Yeap, “Practical low power digital VLSI design”, Kluwer, 1998.
6. Abdelatif Belaouar, Mohamed.I.Elmasry, “Low power digital VLSI design”, Kluwer, 1995.
7. James B.Kulo, Shih-Chia Lin, “Low voltage SOI CMOS VLSI devices and Circuits”, John Wiley and sons, inc. 2001.

Course Outcomes:

On completion of the course the students will be able to

- analyze different sources of power dissipation in CMOS
- implement various power optimization technique at circuit level, architecture level and programming level

14VLE02 VLSI TECHNOLOGY

3 0 0 3

Pre-requisites: Device Modeling

UNIT – I **9**

Crystal growth, wafer preparation, Epitaxy and Oxidation: Electronic Grade Silicon, Czochralski crystal growing, Silicon Shaping, processing consideration, Vapor phase Epitaxy, Molecular Beam Epitaxy, Silicon on Insulators, Growth Mechanism and kinetics, Thin Oxides, Oxidation Techniques and Systems, Oxide properties, Redistribution of Dopants at interface, Oxidation of Poly Silicon, Oxidation induced Defects.

UNIT – II **9**

Lithography and Relative Plasma Etching : Optical Lithography, Electron Lithography, X-Ray Lithography, Ion Lithography, Plasma properties, Feature Size control and Anisotropic Etch mechanism, relative Plasma Etching techniques and Equipments

UNIT – III **9**

Deposition and Diffusion: Deposition process, Polysilicon, Silicon Dioxide- Silicon Nitride- plasma assisted Deposition, Models of Diffusion in Solids, Flick's one dimensional Diffusion Equation – Atomic Diffusion Mechanism –Measurement techniques

UNIT – IV **9**

Ion Implementation and Metallization: Range theory- Implant equipment. Annealing-Shallow junction – High energy implantation – Metallization Applications- Metallization choices- Physical vapor deposition – Patterning

UNIT – V **9**

VLSI Process Integration and Packaging of VLSI Devices: NMOS IC Technology – CMOS IC Technology – MOS Memory IC technology – Bipolar IC Technology – IC Fabrication. Package types– banking design consideration – VLSI assembly technology – Package fabrication technology

TOTAL: 45

REFERENCE BOOKS::

1. Sze, S.M., "VLSI Technology", Second Edition, McGraw-Hill, New York, 1998.
2. Mukherjee, Amar., "Introduction to NMOS and CMOS VLSI System Design", Prentice Hall India, New Delhi, 2000.
3. Plummer, James D., Deal, Michael D. and Griffin, Peter B., "Silicon VLSI Technology: Fundamentals Practice and Modeling", Prentice Hall India, New Delhi, 2000.
4. Chen, Wai Kai., "VLSI Technology", CRC Press, London, 2003.
5. Yurii V Gulyaev and Yu L Kopylov, "VLSI technology: Fundamentals and Applications", 1988 Sov. Phys. Usp.

Course Outcomes:

On completion of the course the students will be able to

- design MOS transistor from wafer preparation
- perform packaging of VLSI ICs

14VLE03 COMPUTER AIDED DESIGN OF VLSI CIRCUITS

3 0 0 3

Pre-requisites: ASIC Design

UNIT – I **9**

Design Methodologies: Introduction to VLSI Design methodologies – Review of VLSI Design automation tools –Algorithmic Graph Theory and Computational Complexity –Tractable and Intractable problems – general purpose methods for combinatorial optimization problems

UNIT – II **9**

Partitioning, Placement and Floor planning : Placement and Partitioning –Circuit representation – Placement algorithms – Partitioning- Partitioning algorithms-Floor planning concepts –shape functions and floor plan sizing –Floor planning based on Simulated Annealing.

UNIT – III **9**

Routing and Compaction: Routing – Types of local routing problems – Area routing – channel routing – global routing –algorithms for global routing. Compaction- Layout Compaction –Design rules –problem formulation –algorithms for constraint graph compaction.

UNIT – IV **9**

Logic Simulation: Simulation –Gate-level modeling and simulation –Switch-level modeling and simulation Combinational Logic Synthesis –Binary Decision Diagrams –ROBDD.

UNIT – V **9**

Logic Synthesis : Two Level Logic Synthesis. High level Synthesis –Hardware models –Internal representation –Allocation assignment and scheduling –Simple scheduling algorithm –Assignment problem –High level transformations

TOTAL: 45

REFERENCE BOOKS::

1. Gerez, S.H., “Algorithms for VLSI Design Automation”, John Wiley & Sons, New York, 2002
2. Sherwani, N.A., “Algorithms for VLSI Physical Design Automation”, Kluwar Academic Publishers, Boston, 2002
3. Sarafzadeh, C.K. Wong, “An Introduction to VLSI Physical Design”, Mc Graw Hill International Edition 1995
4. Hill, D., Shugard, D., Fishburn, J. and Keutzer, K., “Algorithms and Techniques for VLSI Layout Synthesis”, Kluwer Academic Publishers, Boston, 1989
5. Drechsler, R., “Evolutionary Algorithms for VLSI CAD”, Kluwer Academic Publishers, Boston, 1998

Course Outcomes:

On completion of the course the students will be able to

- design ICs using various automation algorithms in IC design process
- analyze various steps involved in the design and fabrication of VLSI chips

14VLE04 INTELLECTUAL PROPERTY BASED VLSI DESIGN

3 0 0 3

Pre-requisites: VLSI Design Techniques

UNIT – I **9**

VLSI and its fabrication: Introduction, IC manufacturing, CMOS technology, IC design techniques, IP based design, Fabrication process-Transistors, Wires and Via, Fabrication Theory reliability, Layout Design and tools.

UNIT – II **9**

Combinational logic networks: Logic Gates: Combinational Logic Functions, Static Complementary Gates, Switch Logic, Alternate Gate circuits, Low power gates, Delay, Yield, Gates as IP, Combinational Logic Networks-Standard Cell based Layout, Combinational network delay, Logic and Interconnect design, Power Optimization, Switch logic network, logic testing

UNIT – III **9**

Subsystem design: Sequential Machine-Latch and Flip flop, System design and Clocking, Performance analysis, power optimization, Design validation and testing; Subsystem Design-Combinational Shifter, Arithmetic Circuits, High Density memory, Image Sensors, FPGA,PLA, Buses and NoC, Data paths, Subsystems as IP.

UNIT – IV **9**

Floor planning and architecture design: Floor planning-Floor planning methods, Global Interconnect, Floor plan design, Off-chip Connections Architecture Design- HDL, Register-Transfer Design, Pipelining, High Level Synthesis, Architecture for Low power, GALS systems, Architecture Testing, IP Components, Design Methodologies, Multiprocessor System-on-chip Design

UNIT – V **9**

Design security: IP in reuse based design, Constrained based IP protection, Protection of data and Privacy constrained based watermarking for VLSI IP based protection

TOTAL: 45

REFERENCE BOOKS::

1. Wayne wolf, "Modern VLSI Design: IP-based Design", Pearson Education, 2009.
2. Qu gang, Miodrag potkonjak, "Intellectual Property Protection in VLSI Designs: Theory and Practice", kluwer academic publishers,2003

Course Outcomes:

On completion of the course the students will be able to

- design the combinational logic network and sequential logic subsystem design using IP
- implement the concepts of floorplanning techniques and architectures

14VLE05 ANALYSIS AND DESIGN OF DIGITAL INTEGRATED CIRCUITS

3 0 0 3

Pre-requisites: VLSI Design Techniques

UNIT – I **9**

Deep submicron digital IC design: Review of Digital Logic Gate Design-digital IC design-computer Aided Design of digital circuits-The MOS Transistor-Bipolar Transistor and circuits-IC Fabrication technology-Layout basics-modeling the MOS transistor for circuit simulation-SPICE MOS level1 device model-BSIM3 model-additional effects in MOS transistors-SOI technology

UNIT – II **9**

MOS inverter circuits, static MOS gate circuits: Voltage transfer characteristics-noise margin definitions-resistive load inverter design-NMOS transistors as load devices-CMOS inverter-pseudo-NMOS inverters-sizing inverters- tristate inverters-CMOS gate circuits-complex CMOS gates-XOR and XNOR gates-multiplexer circuits – Flip-flops and latches – D flip-flops and latches – power dissipation in CMOS gates-power and delay trade-offs

UNIT – III **9**

High speed CMOS logic design, transfer gate and dynamic logic design : Switching time analysis – detailed load capacitance calculation – improving delay calculation with input slope - gate sizing for optimal path delay – optimizing path with logical effort – basic concepts of transfer gate – CMOS transmission gate logic – dynamic D latches and D flip-flops – domino logic –voltage bootstrapping

UNIT – IV **9**

Semiconductor memory and interconnect design : Introduction-MOS decoders – static RAM cell design-SRAM column I/O circuitry – memory architecture-content addressable memories-FPGA-dynamic Read-Write memories-Read Only memories-EPROMs and EEPROMs-flash memory-FRAMs-interconnect RC delays-buffer insertion for very long wires-interconnect coupling capacitance-interconnect inductance-antenna effects.

UNIT – V **9**

Power grid and clock design, low power CMOS logic circuits, chip input and output circuits, design for testability : Power distribution design-clocking and timing issues, phase-locked loops/delay-locked loops – low power design through voltage scaling – estimation and optimization of switching activity – reduction of switched capacitance – adiabatic logic circuits – ESD protection – input circuits – output circuits and L(di/dt) noise – on-chip clock generation and distribution – latch-ups and its prevention – fault types and models – controllability and observability – adhoc testable design techniques – scan based techniques – Built-In-Self Test(BIST) techniques – current monitoring IDDQ test.

TOTAL: 45

REFERENCE BOOKS::

1. Hodges, David A, Jackson, Horace G, and Saleh, Resve A., “Analysis and Design of Digital Integrated Circuits: in deep submicron technology”, Tata McGraw-Hill, New Delhi, 2005.
2. Sung-Mo Kang, and Yusuf Leblebici, “CMOS Digital Integrated Circuits: Analysis and design”, Third Edition, Tata McGraw Hill, New Delhi, 2003.
3. Rabaey, Jan M, Chandrakasan, Anantha, and Borivoje Nikolic, “Digital Integrated Circuits”, Second Edition, Printice Hall Inc, New Jersey, 2006

Course Outcomes:

On completion of the course the students will be able to

- analyse and design high speed, low power CMOS logic design
- design the semiconductor memories

14VLE06 ELECTRONIC DESIGN AUTOMATION TOOLS

3 0 0 3

Pre-requisites: HDL Languages

UNIT – I **9**

Script Language: An overview of OS commands. System settings and configuration. Introduction to Unix commands. Writing Shell scripts

UNIT – II **9**

Synthesis and Simulation: Synthesis and simulation using HDLs-Logic synthesis using verilog and VHDL. Memory and FSM synthesis. Performance driven synthesis, Simulation- Types of simulation. Static timing analysis. Formal verification. Switch level and transistor level simulation.

UNIT – III **9**

Circuit simulation using SPICE – circuit description. AC, DC and transient analysis. Advanced spice commands and analysis. Models for diodes, transistors and opamp. Digital building blocks. A/D, D/A and sample and hold circuits. Design and analysis of mixed signal circuits.

UNIT – IV **9**

VLSI design automation tools. An overview of the features of practical CAD tools. Modelsim, Leonardo spectrum, Xilinx, Quartus II, VLSI backend tools. Mixed signal circuit modeling and analysis using VHDL –AMS, Synopsys.

UNIT – V **9**

System Design: System design using systemC- System C models of computation. Classical hardware modeling in system C. Functional modeling. Parametrized modules and channels. Test benches. Tracing and debugging.

TOTAL: 45

REFERENCE BOOKS::

1. M.J.S.Smith, Application Specific Integrated Circuits,Pearson,2002
2. M.H.Rashid, Spice for Circuits and Electronics using Pspice. (2/e), PHI
3. T. Grdtker et al , System Design with SystemC, Kluwer, 2004.
4. P.J. Ashenden et al , The System Designer's Guide to VHDL-AMS, Elsevier, 2005
5. www.semiconductorsimulation.com

Course Outcomes:

On completion of the course the students will be able to

- explore simulation tools and synthesis concepts for digital circuits
- develop mixed Signal Circuits

14VLE07 OPTIMIZATION TECHNIQUES FOR VLSI CIRCUITS

3 0 0 3

Pre-requisites: Advanced Mathematics

UNIT – I **9**

Linear Programming Problem: Mathematical Formulation – Basic definitions – Solutions of LPP: Graphical method, Simplex method –Big–M method and Two phase method – Duality theory – Dual simplex method.

UNIT – II **9**

Transportation Model and Assignment Model: Mathematical Formulation – Methods for finding Initial Basic Feasible Solution – MODI method – Degeneracy in transportation problem – Unbalanced transportation problems – Maximization case in transportation problem. **Assignment Model** :Mathematical Formulation – Hungarian algorithm – Unbalanced assignment problem – Maximization case in assignment model.

UNIT – III **9**

Non-Linear Programming: Formulation of non–linear programming problem – Constrained optimization with equality constraints – Constrained optimization with inequality constraints – Graphical method of non–linear programming problem involving only two variables – Kuhn-tucker conditions with non-negative constraints.

UNIT – IV **9**

Replacement Model: Introduction - Replacement of Items that Deteriorate – Replacement of Items that Fail Suddenly – Group Replacement policy.

UNIT – V **9**

Dynamic programming: Principle of optimality – Recursive equation approach – Application to shortest route, Cargo-loading, Allocation and Production schedule problems.

TOTAL: 45

REFERENCE BOOKS::

1. Kanti Swarup Gupta, P.K and Man Mohan “Operations Research”, S.Chand & Co., 1997.
2. Trembly J.P and Manohar R, “Discrete Mathematical Structures with Applications to Computer Science”, Tata McGraw–Hill, New Delhi, 2008.
3. Kapur, J.N. and Saxena, H.C., “Mathematical Statistics”, S.Chand & Co., New Delhi, 2007.
4. Taha, H.A., “Operations Research- An Introduction”, 6th Edition, Prentice Hall of India, 2008.
5. www.elsevierdirect.com

Course Outcomes:

On completion of the course the students will be able to

- implement different techniques for solving optimization problems
- construct models to handle the complicated problems

14VLE08 RECONFIGURABLE ARCHITECTURES FOR VLSI

3 0 0 3

Pre-requisites: HDL for IC design

UNIT – I **9**

Device architecture: General Purpose Computing Vs Reconfigurable Computing – Simple Programmable Logic Devices– Complex Programmable Logic Devices – FPGAs – Device Architecture - Case Studies.

UNIT – II **9**

Reconfigurable computing architectures and systems: Reconfigurable Processing Fabric Architectures – RPF Integration into Traditional Computing Systems – Reconfigurable Computing Systems – Case Studies – Reconfiguration Management

UNIT – III **9**

Programming reconfigurable systems: Compute Models - Programming FPGA Applications in HDL – Compiling C for Spatial Computing – Operating System Support for Reconfigurable Computing

UNIT – IV **9**

Mapping designs to reconfigurable platforms: The Design Flow - Technology Mapping – FPGA Placement and Routing – Configuration Bit stream Generation – Case Studies with Appropriate Tools.

UNIT – V **9**

Application development with FPGAs: Case Studies of FPGA Applications – System on a Programmable Chip (SoPC) Designs

TOTAL: 45

REFERENCE BOOKS::

1. Maya B. Gokhale and Paul S. Graham, "Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays", Springer, 2005
2. Scott Hauck and Andre Dehon (Eds.), "Reconfigurable Computing – The Theory and Practice of FPGA-Based Computation", Elsevier / Morgan Kaufmann, 2008.
3. Christophe Bobda, "Introduction to Reconfigurable Computing – Architectures, Algorithms and Applications", Springer, 2010.

Course Outcomes:

On completion of the course the students will be able to

- understand the reconfigurable computing architecture and systems
- place and route the different blocks

14VLE09 RF VLSI DESIGN

3 0 0 3

Pre-requisites: VLSI Design Techniques

UNIT – I **9**

CMOS physics, transceiver specifications and architectures: Introduction to MOSFET Physics, Noise: Thermal, shot, flicker, popcorn noise, Two port Noise theory, Noise Figure, THD, IP2, IP3, Sensitivity, SFDR, Phase noise - Specification distribution over a communication link, Homodyne Receiver, Heterodyne Receiver, Image reject, Low IF Receiver Architectures Direct up conversion Transmitter, Two step up conversion Transmitter

UNIT – II **9**

Impedance matching and amplifiers: S-parameters with Smith chart, Passive IC components, Impedance matching networks, Common Gate, Common Source Amplifiers, OC Time constants in bandwidth estimation and enhancement, High frequency amplifier design, Power match and Noise match, Single ended and Differential LNAs, Terminated with Resistors and Source Degeneration LNAs.

UNIT – III **9**

Feedback systems and power amplifiers : Stability of feedback systems: Gain and phase margin, Root-locus techniques, Time and Frequency domain considerations, Compensation, General model – Class A, AB, B, C, D, E and F amplifiers, Power amplifier Linearization Techniques, Efficiency boosting techniques, ACPR metric, Design considerations

UNIT – IV **9**

Mixers and oscillators: Mixer characteristics, Non-linear based mixers, Quadratic mixers, Multiplier based mixers, Single balanced and double balanced mixers, subsampling mixers, Oscillators describing Functions, Colpitts oscillators Resonators, Tuned Oscillators, Negative resistance oscillators, Phase noise.

UNIT – V **9**

PLL and frequency synthesizers: Linearised Model, Noise properties, Phase detectors, Loop filters and Charge pumps, Integer-N frequency synthesizers, Direct Digital Frequency synthesizers

TOTAL: 45

REFERENCE BOOKS::

1. T.Lee, “Design of CMOS RF Integrated Circuits”, Cambridge, 2004.
2. B.Razavi, “RF Microelectronics”, Pearson Education, 1997.
3. Jan Crols, Michiel Steyaert, “CMOS Wireless Transceiver Design”, Kluwer Academic Publishers,1997.
4. B.Razavi, “Design of Analog CMOS Integrated Circuits”, McGraw Hill, 2001
5. http://www.ee.iitm.ac.in/~ani/ee6240/

Course Outcomes:

On completion of the course the students will be able to

- explore the principle and operation of RF design blocks
- design CMOS RF front end and high frequency wireline systems

14VLE10 NANO ELECTRONICS

3 0 0 3

Pre-requisites: Device Modeling

UNIT – I **9**

CMOS scaling challenges in Nanoscale regimes : Leakage current mechanisms in nanoscale CMOS, leakage control and reduction techniques, process variations in devices and interconnects. **Device technologies for sub 100nm CMOS:** Silicidation and Cu-low k interconnects, strain silicon – biaxial stain and process induced strain; Metal-high k gate; Emerging CMOS technologies at 32nm scale and beyond – FINFETs, surround gate nanowire MOSFETs, heterostructure (III-V) and Si-Ge MOSFETs

UNIT – II **9**

Device scaling and ballistic MOSFET: Two dimensional scaling theory of single and multigate MOSFETs, generalized scale length, quantum confinement and tunneling in MOSFTEs, velocity saturation, carrier back scattering and injection velocity effects, scattering theory of MOSFETs

UNIT – III **9**

Emerging Nanoscale devices: Si and hetero-structure nanowire MOSFETs, carbon nanotube MOSFETs, quantum wells, quantum wires and quantum dots; Single electron transistors, resonant tunneling devices

UNIT – IV **9**

Nanoscale CMOS design: CMOS logic power and performance, voltage scaling issues; Introduction to low power design; Performance optimization for data paths

UNIT – V **9**

Nanoscale circuits : Statistical circuit design, variability reduction, design for manufacturing and design optimization; Sequential logic circuits, registers, timing and clock distribution, IO circuits and memory design and trends.

Non-classical CMOS: CMOS circuit design using non-classical devices – FINFETs, nanowire, carbon nanotubes and tunnel devices.

TOTAL: 45

REFERENCE BOOKS::

1. Lundstrom, M., "Nanoscale Transport: Device Physics, Modeling, and Simulation", Springer. 2000
2. Maiti, C.K., Chattopadhyay, S. and Bera, L.K., "Strained-Si and Hetrostructure Field Effect Devices", Taylor and Francis, 2007
3. Hanson, G.W., "Fundamentals of Nanoelectronics", Pearson, India., 2008.
4. Wong, B.P., Mittal, A., Cao Y. and Starr, G., "Nano-CMOS Circuit and Physical Design", Wiley, 2004
5. Lavagno, L., Scheffer, L. and Martin, G., "EDA for IC Implementation Circuit Design and Process Technology", Taylor and Francis, 2005

Course Outcomes:

On completion of the course the students will be able to

- design nano circuits with low power design concepts and scaling techniques
- design nano classical CMOS devices

14MME03 MEMS DESIGN

(Common to Mechatronis, Applied Electronics, Control and Instrumentation Engineering & VLSI Design)

3 0 0 3

Pre requisites: Sensors and Instrumentation, Bridge course mechanical

UNIT – I **9**

Materials for MEMS and Scaling Laws: Overview - Microsystems and microelectronics - Working principle of Microsystems – Si as a substrate material - Mechanical properties - Silicon compounds - Silicon piezoresistors - Gallium aresenside - Quartz-piezoelectric crystals - Polymer -Scaling laws in Miniaturization.

UNIT – II **9**

Micro Sensors, Micro Actuators: Micro sensors – Types- Micro actuation techniques- Microactuators – Micromotors – Microvalves – Microgrippers – Micro accelerometer – introduction – Types - Actuating Principles, Design rules ,modeling and simulation, Verification and testing –Applications- Fundamentals of micro fluidics- Micro-pump- Types, Actuating Principles, Design rules ,modeling and simulation, Verification and testing –Applications

UNIT – III **9**

Mechanics for Microsystem Design: Static bending of thin plates - Mechanical vibration - Thermo mechanics - Thermal stresses - Fracture mechanics - Stress intensity factors, fracture toughness and interfacial fracture mechanics-Thin film Mechanics-Overview of Finite Element Stress Analysis.

UNIT – IV **9**

Fabrication Process and Micromachining: Photolithography - Ion implantation - Diffusion – Oxidation – CVD - Physical vapor deposition - Deposition by epitaxy - Etching process- Bulk Micro manufacturing - Surface micro machining – LIGA –SLIGA.

UNIT – V **9**

Micro System Design, Packaging and Applications: Design considerations - Process design - Mechanical design – Mechanical Design using Finite Element Method-Micro system packaging – Die level - Device level - System level – Packaging techniques - Die preparation - Surface bonding - Wire bonding – Sealing – CAD tools to design a MEMS device- Applications of micro system in Automotive industry, Bio medical, Aerospace and Telecommunications.

TOTAL : 45

REFERENCE BOOKS:

1. Mohamed Gad-el-Hak, "The MEMS Hand book", CRC press, 2009.
2. Tai-Ran Hsu, "MEMS and Microsystems Design and Manufacture", Tata McGraw-Hill, New Delhi, 2008.
3. M.-H. Bao, "Micromechanical Transducers: Pressure sensors, accelrometers, and gyroscopes", Elsevier, New York, 2000.
4. Julian W. Gardner, Vijay K. Varadan, Osama and Awadel Karim, O., "Microsensors MEMS and Smart Devices", John Wiley & sons Ltd., New York, 2001.
5. Tai---Ran Hsu, "MEMS & Microsystems: Design, Manufacture, and Nanoscale Engineering", 2nd Edition, Wiley & Sons ISBN: 978---0---470---08301---7, March 2008.

6. Chang Liu, “Foundations of MEMS”, Prentice Hall, 2006.
7. IEEE/ASME: Journal on Microelectromechanical Systems.

Course Outcomes:

On completion of the course the students will be able to

- understand the basic concepts of microsensors, microactuators and micromechanics
- know the microfabrication and micromanufacturing techniques
- apply the knowledge to design a microsystem for various applications

14COE16 ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY

(Common to Communication Systems, VLSI Design, Applied Electronics & Control and Instrumentation Engineering)

3 0 0 3

Pre-requisites: Microwave Communication

UNIT – I **9**

EMI Environment : EMI/EMC concepts and definitions, Sources of EMI, conducted and radiated EMI, Transient EMI, Time domain Vs Frequency domain EMI, Units of measurement parameters, Emission and immunity concepts, ESD

UNIT – II **9**

EMI Coupling Principles: Conducted, Radiated and Transient Coupling, Common Impedance Ground Coupling, Radiated Common Mode and Ground Loop Coupling, Radiated Differential Mode Coupling, Near Field Cable to Cable Coupling, Power Mains and Power Supply coupling

UNIT – III **9**

EMI/EMC standards and measurements : Civilian standards - FCC, CISPR,I EC, EN, Military standards - MIL STD 461D/462, EMI Test Instruments /Systems, EMI Shielded Chamber, Open Area Test Site, TEM Cell, Sensors/Injectors/Couplers, Test beds for ESD and EFT, Military Test Method and Procedures (462).

UNIT – IV **9**

EMI control techniques : Shielding, Filtering, Grounding, Bonding, Isolation Transformer, Transient Suppressors, Cable Routing, Signal Control, Component Selection and Mounting

UNIT – V **9**

EMC design of PCBs : PCB Traces Cross Talk, Impedance Control, Power Distribution Decoupling, Zoning, Motherboard Designs and Propagation Delay Performance Models

TOTAL : 45

REFERENCE BOOKS:

1. Ott, Henry W., "Noise Reduction Techniques in Electronic Systems", John Wiley & Sons, New York, 1988
2. Paul, C.R., “Introduction to Electromagnetic Compatibility”, John Wiley & Sons, New York, 1992
3. Kodali, V.P., "Engineering EMC Principles, Measurements and Technologies", IEEE Press, London, 1996.
4. Keiser, Bernhard., "Principles of Electromagnetic Compatibility", Third Edition, Artech House, Dedham, 1986.

Course Outcomes:

On completion of the course the students will be able to

- formulate the various aspects EMI/EMC coupling
- identify a suitable EMI testing and controlling techniques
- develop the EMC design of PCBs

14VLE11 DESIGN OF SEMICONDUCTOR MEMORIES

3 0 0 3

Pre-requisites: Digital Electronics

UNIT – I **9**

Random access memory technologies: SRAM Cell Structures-MOS SRAM Architecture-MOS SRAM Cell and Peripheral Circuit Operation-BipolarSRAM Technologies-Silicon On Insulator (SOl) Technology-Advanced SRAM Architectures and Technologies-Application Specific SRAMs DRAM Technology Development-CMOS DRAMs-DRAMs Cell Theory and Advanced Cell Strucutures-BiCMOS,DRAMs-Soft Error Failures in DRAMs-Advanced DRAM Designs and Architecture-Application Specific DRAMs

UNIT – II **9**

Nonvolatile memories : Masked Read-Only Memories (ROMs)-High Density ROMs-Programmable Read-Only Memories (PROMs)-BipolarPROMs-CMOS PROMs-Erasable (UV) - Programmable Road-Only Memories (EPROMs)-Floating-GateEPROM Cell-One-Time Programmable (OTP) Eproms-Electrically Erasable PROMs (EEPROMs)-EEPROM Technology And Arcitecture-Nonvolatile SRAM-Flash Memories (EPROMs or EEPROM)-AdvancedFlash Memory Architecture.

UNIT – III **9**

Memory fault modeling and testing: RAM Fault Modeling, Electrical Testing, Peusdo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory Testing.

UNIT – IV **9**

Semiconductor memory reliability : General Reliability Issues-RAM Failure Modes and Mechanism-Nonvolatile Memory Reliability-Reliability Modeling and Failure Rate Prediction-Design for Reliability-Reliability Test Structures-Reliability Screening and Qualification.

UNIT – V **9**

Packaging technologies : Radiation Effects-Single Event Phenomenon (SEP)-Radiation Hardening Techniques-Radiation Hardening Process and Design Issues-Radiation Hardened Memory Characteristics-Radiation Hardness Assurance and Testing - Radiation Dosimetry-Water Level Radiation Testing and Test Structures. Ferroelectric Random Access Memories (FRAMs)-Gallium Arsenide (GaAs) FRAMs-Analog Memories-Magnetoresistive Random Access Memories (MRAMs)-Experimental Memory Devices. Memory Hybrids and MCMs (2D)-Memory Stacks and MCMs (3D)-Memory MCM Testing and Reliability Issues-Memory Cards-High Density Memory Packaging Future Directions**:**

TOTAL: 45

REFERENCE BOOKS::

1. Sharma, Ashok K., “Semiconductor Memories: Technology, Testing, and Reliability”, Wiley-IEEE Press, New York, 2002
2. Sharma, Ashok K., “Semiconductor Memories”, Two-Volume Set**,** Wiley-IEEE Press, New York, 2003.
3. Betty Prince, “Emerging Memories: Technologies and Trends” Kluwer Academic Publishers, 2002.

Course Outcomes:

On completion of the course the students will be able to

- explore memory cell architectures and operation
- design memory and apply test algorithms

14VLE12 DSP PROCESSOR ARCHITECTURE AND PROGRAMMING

(Common to VLSI Design & Communication Systems)

3 0 0 3

Pre-requisites: Digital Signal Processing.

UNIT – I **9**

Fundamentals of programmable DSPs: Multiplier and Multiplier accumulator (MAC) – Modified Bus Structures and Memory access in Programmable DSPs – Multiple access memory – Multi-port memory – VLIW architecture- Pipelining – Special Addressing modes in P-DSPs – On chip Peripherals

UNIT – II **9**

TMS320C54XX: Fundamentals of Programmable DSPs - Architecture of TMS320C54X-54X Buses-Memory organization-Computational Units-Pipeline operation-On-chip peripherals –Address Generation Units- Addressing modes and instruction set- assembly language instructions -Introduction to Code Composer studio

UNIT – III **9**

TMS320C6X : Architecture of TMS320C6X – Computational units-Addressing modes –Memory architecture- pipeline operation- instruction set- assembly language instructions

UNIT – IV **9**

Blackfin Processor(BF537): Architecture of BF537- Computational units - Internal Memory organization- System interrupts – Direct Memory Access- on-chip peripherals-ALU-MAC-DAG Units-Addressing modes-Assembly language instructions- Timers –Interrupts-Serial ports-UART-Simple programs

UNIT – V **9**

Applications Using TMS320C54X/C6X/BF537: Program development - Software Development Tools- The Assembler and the Assembly Source File Filter design- Linker and Memory Allocation - DSP Software Development Steps- Speech Digitization-Encoding & Decoding-Image compression-Restoration-Adaptive Echo cancellation-Modulation

TOTAL: 45

REFERENCE BOOKS::

1. Venkataramani, B. and Bhaskar, M., "Digital Signal Processors: Architecture, Programming and Applications", Tata McGraw–Hill, New Delhi, 2003
2. Texas Instrumentation, "User guides: Analog Devices", Motorola Inc, Arizona, 2003
3. Sen.M.Kuo, Woon–Seng S.Gan, "Digital Signal Processors: Architecture, Implementation and Applications", Prentice Hall, 2005
4. www.analogdevices.com.

Course Outcomes:

On completion of the course the students will be able to

- utilize the architecture of various DSP processor
- design various applications using DSP processors

14VLE13 GENETIC ALGORITHMS

3 0 0 3

UNIT – I **9**

Introduction, GA Technology-Steady State Algorithm-Fitness Scaling-Inversion

UNIT – II **9**

GA for VLSI Design, Layout and Test automation-partitioning- automatic placement, routing technology, Mapping for FPGA -Automatic test generation-Partitioning algorithm Taxonomy - Multiway Partitioning.

UNIT – III **9**

Hybrid genetic – genetic encoding-local improvement-WDFR-Comparison of Cas-Standard cell placement-GASP algorithm-unified algorithm.

UNIT – IV **9**

Global routing-FPGA technology mapping-circuit generation-test generation in a GA frame work-test generation procedures

UNIT – V **9**

Power estimation-application of GA-Standard cell placement-GA for ATG-problem encoding- fitness function-GA vs Conventional algorithm.

TOTAL: 45

REFERENCE BOOKS::

1. Pinaki Mazumder,E.MRudnick,"Genetic Algorithm for VLSI Design,Layout and test Automation", Prentice Hall,1998.
2. Randy L. Haupt, Sue Ellen Haupt, "Practical Genetic Algorithms" Wiley – Interscience, 1977
3. Ricardo Sal Zebulum, Macro Aurelio Pacheco, Marley Maria B.R. Vellasco, Marley Maria Bernard Vellasco "Evolution Electronics: Automatic Design of electronic Circuits and Systems Genetic Algorithms", CRC press, 1st Edition Dec 2001.
4. John R.Koza, Forrest H.Bennett III, David Andre , Morgan Kufmann, "Genetic Programming Automatic programming and Automatic Circuit Synthesis", 1st Edition , May 1999

Course Outcomes:

On completion of the course the students will be able to

- utilize the concept of Genetic algorithm for VLSI circuits
- implement the Genetic algorithm for automation of partitioning, routing, placement and test automation

14VLE14 SUBMICRON VLSI DESIGN

3 0 0 3

Pre-requisites: VLSI Design

UNIT – I **9**

SILICON REALIZATION OF ASIC : Introduction-Handcrafted layout implementation-bit-slice layout implementation-Cell based layout implementation- gate array layout implementation-Hierchial design approach- The choice of layout implementation form

UNIT – II **9**

LOW POWER DESIGN : Sources of CMOS power consumption-technology options for low power-reduction of P-leak by technological measures Reduction of P-dyn by technology measures-reduction of P-dyn by reduced voltage process-design option for low power-computing power vs chip power-a scaling perspectives.

UNIT – III **9**

DESIGN FOR RELIABILITY : Introduction-latch up in CMOS circuits-Electrostatics discharge-and its protection-Electro migration- Hot carrier degradation design for signal integrity-clock distribution and critical timing issues-clock generation and synchronization in different domain on a chip-the influence of interconnection design organization

UNIT – IV **9**

DEEP SUB MICRON :RF CMOS Transistor downsizing limitations-. RF basic blocks layout implementation Submicron technology and layout dependent effects-input output interfacing, the bonding pad, the pad ring, electrostatic discharge prevention

UNIT – V **9**

CMOS DEVICES : Clamp CMOS devices, zener diode-input structure-output structure-pull up-pull down-i/o pad, power clamp-core/pad limitation I/O Pad description using Ibis-Connecting to the package-Signal propagation between integrated circuits

TOTAL: 45

REFERENCE BOOKS::

1. Deep-Submicron Cmos Ics: From Basics to Asics By Harry J. M. Veendrick
2. Low Power Design in Deep Submicron Electronics by W. Nebel, Jean P. Mermet
3. Low-Power Deep Sub-Micron CMOS Logic: Sub-threshold Current Reduction by P.R. Van Der Meer, Arie van Staveren, Arthur H. M. van Roermund

Course Outcomes:

On completion of the course the students will be able to

- design low power ASIC and CMOS devices at deep submicron level
- implement RF CMOS transistor sizing

14VLE15 VLSI FOR WIRELESS COMMUNICATION

3 0 0 3

Pre-requisites: VLSI Design Techniques

UNIT – I **9**

Components and Devices : Integrated inductors, resistors, MOSFET and BJT AMPLIFIER DESIGN: Low Noise Amplifier Design - Wideband LNA - Design Narrowband LNA - Impedance Matching - Automatic Gain Control Amplifiers – Power Amplifiers

UNIT – II **9**

Mixers : Balancing Mixer - Qualitative Description of the Gilbert Mixer - Conversion Gain – Distortion – Low Frequency Case: Analysis of Gilbert Mixer – Distortion - High-Frequency Case – Noise – A Complete Active Mixer. Switching Mixer - Distortion in Unbalanced Switching Mixer – Conversion Gain in Unbalanced Switching Mixer - Noise in Unbalanced Switching Mixer - A Practical Unbalanced Switching Mixer. Sampling Mixer - Conversion Gain in Single Ended Sampling Mixer - Distortion in Single Ended Sampling Mixer - Intrinsic Noise in Single Ended Sampling Mixer - Extrinsic Noise in Single Ended Sampling Mixer.

UNIT – III **9**

Frequency Synthesizers : Phase Locked Loops - Voltage Controlled Oscillators - Phase Detector – Analog Phase Detectors – Digital Phase Detectors - Frequency Dividers - LC Oscillators - Ring Oscillators - Phase Noise - A Complete Synthesizer Design Example (DECT Application).

UNIT – IV **9**

UB Systems : Data converters in communications, adaptive Filters, equalizers and transceivers

UNIT – V **9**

Implementations : VLSI architecture for Multitier Wireless System - Hardware Design Issues for a Next generation CDMA System.

TOTAL: 45

REFERENCE BOOKS::

1. B.Razavi ,"RF Microelectronics" , Prentice-Hall ,1998.
2. Bosco H Leung "VLSI for Wireless Communication", Pearson Education, 2002.
3. Thomas H.Lee, "The Design of CMOS Radio –Frequency Integrated Circuits', Cambridge University Press ,2003.
4. Emad N Farag and Mohamed I Elmasry, "Mixed Signal VLSI Wireless Design - Circuits and Systems", Kluwer Academic Publishers, 2000.
5. Behzad Razavi, "Design of Analog CMOS Integrated Circuits" McGraw –Hill, 1999.
6. J. Crols and M. Steyaert, "CMOS Wireless Transceiver Design," Boston, Kluwer Academic Pub., 1997.

Course Outcomes:

On completion of the course the students will be able to

- design low noise amplifiers and mixers for wireless communication
- design PLL and VCO
- implement the concepts of CDMA in wireless communication

14VLE16 HARDWARE SOFTWARE CO-DESIGN

3 0 0 3

Pre-requisites: ASIC Design

UNIT – I **9**

System Specification and Modeling : Embedded Systems, Hardware/Software Co-Design, Co - Design for System Specification and Modelling, Co - Design for Heterogeneous Implementation - Processor Synthesis, Single – Processor Architectures with one ASIC, Single-Processor Architectures with many ASICs, Multi- Processor Architectures, Comparison of Co- Design Approaches, Models of Computation , Requirements for Embedded System Specification .

UNIT – II **9**

Hardware/Software Partitioning: The Hardware/Software Partitioning Problem, Hardware-Software Cost Estimation, Generation of the Partitioning Graph, Formulation of the HW/SW Partitioning Problem , Optimization , HW/SW Partitioning based on Heuristic Scheduling, HW/SW Partitioning based on Genetic Algorithms .

UNIT – III **9**

Hardware/Software Co-Synthesis : The Co - Synthesis Problem, State - Transition Graph, Refinement and Controller Generation, Distributed System Co-Synthesis

UNIT – IV **9**

Prototyping and Emulation : Introduction, Prototyping and Emulation Techniques , Prototyping and Emulation Environments ,Future Developments in Emulation and Prototyping, Target Architecture-Architecture Specialization Techniques ,System Communication Infrastructure, Target Architectures and Application System Classes, Architectures for Control-Dominated Systems, Architectures for Data-Dominated Systems ,Mixed Systems and Less Specialized Systems

UNIT – V **9**

Design Specification and Verification : Concurrency, Coordinating Concurrent Computations, Interfacing Components, Verification, Languages for System-Level Specification and Design System - Level Specification ,Design Representation for System Level Synthesis, System Level Specification Languages, Heterogeneous Specification and Multi-Language Co- simulation

TOTAL: 45

REFERENCE BOOKS::

1. Ralf Niemann, “Hardware/Software Co-Design for Data Flow Dominated Embedded Systems”, Kluwer Academic Pub, 1998.
2. Jorgen Staunstrup, Wayne Wolf ,”Hardware/Software Co-Design: Principles and Practice” , Kluwer Academic Pub, 1997
3. Giovanni De Micheli, Rolf Ernst Morgon,” Reading in Hardware/Software Co-Design“, Kaufmann Publishers, 2001.

Course Outcomes:

On completion of the course the students will be able to

- design the co-design approaches for single processor and multiprocessor architectures
- utilize various techniques of prototyping and emulation for co-design
- implement the languages for system level specification and design

14COE05 DIGITAL IMAGE PROCESSING AND MULTI RESOLUTION ANALYSIS

(Common to Communication Systems, VLSI Design, Embedded Systems, Computer and Communication Engineering & Mechatronics)

3 0 0 3

Pre-requisites: Digital Signal Processing

UNIT – I **9**

Image Transforms: Orthogonal transforms – FT,DST,DCT, Hartley, Walsh hadamard, Haar, Radon, Slant Wavelet, KL, SVD and their properties

UNIT – II **9**

Image Enhancement and Restoration: Image enhancement - Point operations - contrast stretching - clipping and thresholding - digital negative intensity level slicing - bit extraction. Histogram processing - histogram equalisation -modification. Spatial operations – smoothing spatial filters, sharpening spatial filters. Transform operations. Color image enhancement. Image Restoration – degradation model, Noise models, Unconstrained and Constrained restoration, Inverse filtering – removal of blur caused by uniform linear motion, Wiener filtering, Restoration by SVD and Homomorphic filtering

UNIT – III **9**

Image Compression: Image Compression – Need for data compression – Run length encoding – Huffman coding – Arithmetic coding – predictive coding- transform based compression, - vector quantization – block truncation coding.

Image Segmentation: Point, Edge and line detection -thresholding-Region based approach

Image Representation: boundary based – region based and intensity based description

UNIT – IV **9**

Registration and Multi valued image Processing: Registration – geometric transformation – registration by mutual information

Mutivalued image processing – colour image processing – colour image enhancement- satellite image processing- radiometric correction – other errors- multi spectral image enhancement- medical image processing – image fusion

UNIT – V **9**

Wavelets And Multiresolution Processing : Image Pyramids – Subband coding – The Haar Transform – Multiresolution Expansion – Series Expansion – Scaling Function – Wavelet Function – Wavelet Transform in One Dimension- The Wavelet Series Expansion – The Discrete Wavelet Transform – The Continuous Wavelet Transform – The Fast Wavelet Transform – Wavelet transform in two dimensions– Applications in image denoising and compression

Total : 45

REFERENCE BOOKS:

1. Chanda B, Dutta Majumder D., “Digital Image Processing and analysis”, 2nd Edition, PHI learning, 2011
2. Gonzalez, Rafel C. and Woods, Richard E., "Digital Image Processing", 2nd Edition, Prentice Hall, New York, 2006.

3. Jain, Anil K., "Fundamentals of Digital Image Processing", Prentice Hall of India, New Delhi, 2003.
4. Rosenfield, Azriel and Kak, Avinash C., “Digital Picture Processing”, Academic Press Inc, New York, 1982.
5. Jayaraman. S, Esakkirajan. S, and Veerakumar. T, “Digital Image Processing” Tata McGraw-Hill, New Delhi, 2009

Course Outcomes:

On completion of the course the students will be able to

- analyze and process digital images and color images in various domains
- apply concepts of wavelets in image processing for various applications

14COT11 STATISTICAL SIGNAL PROCESSING

(Common to Communication Systems, VLSI Design, Embedded Systems & Computer and Communication Engineering)

3 1 0 4

Pre-requisites: Digital Signal Processing

UNIT – I **9**

Discrete Random Signal Processing: Discrete time random process – Random process: Ensemble averages- Gaussian process – stationary process – The autocovariance and autocorrelation matrices – ergodicity – white noise the power spectrum. Filtering random process – spectral factorization. Parseval's theorem – Wiener Khintchine relation.

UNIT – II **9**

Spectrum Estimation and Analysis: Non parametric methods: Periodogram, performance of periodogram, modified periodogram, Bartlett's method, Welch's method.

Parametric methods: AR model – Yule-Walker method, MA model – ARMA model.

UNIT – III **9**

Linear Prediction: Forward and backward linear predictions, Solution of the normal equations – Levinson-Durbin algorithms. Least mean squared error criterion – The FIR Wiener filter – filtering – linear prediction and The IIR Wiener filters – Non causal IIR Wiener filter – the causal IIR Wiener filter.

UNIT – IV **9**

Adaptive Filter: Concepts of adaptive filter – FIR adaptive filters – LMS algorithm – Applications: Noise cancellation-Adaptive recursive filers– AR lattice structure and ARMA process, lattice – ladder filters.

UNIT – V **9**

Overview of speech processing : Speech Fundamentals: Articulatory Phonetics – Production and Classification of Speech Sounds; Acoustic Phonetics – acoustics of speech production; Short time Homomorphic Filtering of Speech; Linear Prediction (LP) analysis: Basis and development, LPC spectrum.

Lecture: 45, Tutorial: 15, TOTAL: 60

REFERENCE BOOKS:

1. Hayes, Monson H. "Statistical Digital Signal processing and Modeling", John Wiley and Sons, Inc., 1996
2. Proakis, John G. and Manolakis, Dimitris G. "Digital Signal Processing: Principles Algorithms and Applications", PHI, 2006.
3. Ifeachor, Emmanuel C. and Jervis, Barrie N. "Digital Signal Processing: A Practical Approach", Addison-Wesley Publishing Company, 2002.

Course Outcomes:

On completion of the course the students will be able to

- demonstrate the concepts of discrete random signal processing in real time applications
- estimate and analyze the spectrum using parametric and non-parametric approach
- design an adaptive filter and various error minimization algorithm for speech quality improvement