KONGU ENGINEERING COLLEGE
PERUNDURAI ERODE – 638 060
(Autonomous)

VISION

To be a centre of excellence for development and dissemination of knowledge in Applied Sciences, Technology, Engineering and Management for the Nation and beyond.

MISSION

We are committed to value based Education, Research and Consultancy in Engineering and Management and to bring out technically competent, ethically strong and quality professionals to keep our Nation ahead in the competitive knowledge intensive world.

QUALITY POLICY

We are committed to

- Provide value based quality education for the development of students as competent and responsible citizens.
- Contribute to the nation and beyond through research and development
- Continuously improve our services

DEPARTMENT OF EEE

VISION

To be a centre of excellence for development and dissemination of knowledge in Electrical and Electronics Engineering to benefit the society in the national and global level.

MISSION

Department of Electrical and Electronics Engineering is committed to:

MS1: Develop innovative, competent, ethical and quality engineers to contribute for technical advancements to meet societal needs.

MS2: Provide state-of-the-art facilities for continual improvement in teaching-learning process and research activities.

MS3: Enrich the knowledge and skill of the students to cater to the industrial needs and motivate them to become entrepreneurs.

2018 REGULATIONS

PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

Graduates of **Applied Electronics** will

PEO1: Apply fundamental knowledge of electronics in related fields to succeed in professional and research career.

PEO2: Design, simulate, analyze and develop electronics engineering based products that are cost efficient, reliable and safe.

PEO3: Exhibit proficiency, ethical outlook, communication skills and adopt to current trends through lifelong learning.

MAPPING OF MISSION STATEMENTS (MS) WITH PEOs

MS\PEO	PEO1	PEO2	PEO3
MS1	3	3	2
MS2	2	2	2
MS3	3	3	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

PROGRAM OUTCOMES (POs)	
Post Graduates of Applied Electronics will have	
PO1	An ability to independently carry out research /investigation and development work to solve practical problems
PO2	An ability to write and present a substantial technical report/document
PO3	An ability to demonstrate a degree of mastery over the area of applied electronics.

MAPPING OF PEOs WITH POs

PEO\PO	PO1	PO2	PO3
PEO1	3	1	2
PEO2	3	1	3
PEO3	3	2	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

CURRICULUM BREAKDOWN STRUCTURE UNDER REGULATION 2018

Curriculum Breakdown Structure(CBS)	Curriculum Content (% of total number of credits of the program)	Total number of contact hours	Total number of credits
Program Core(PC)	41.66	495	30
Program Electives(PE)	25	270	18
Humanities and Social Sciences and Management Studies(HSMS)	5.55	60	4
Project(s)/Internships(PR)/Others	27.77	600	20
Total			**72**

KEC R2018: SCHEDULING OF COURSES – ME APPLIED ELECTRONICS

Semester	Theory/ Theory cum Practical / Practical						Internship & Projects	Special Courses	Credits
	1	2	3	4	5	6	7	8	9
I	18AMT14 Advanced Mathematics for Electrical Engineers (HS-3-1-0-4)	18PET11 System Theory (PC-3-1-0-4)	18AET11 Modern Digital Signal Processing (PC-3-1-0-4)	18AET12 CMOS VLSI Design (PC-3-0-0-3)	18AET13 Computational Intelligence Techniques (PC-3-0-0-3)	18AEC11 Embedded Systems (PC-3-0-2-4)			22
II	18AEC21 Design of Analog Integrated Circuits (PC-3-0-2-4)	18AEC22 Digital System Design (PC-3-0-2-4)	18VLE03 Low Power Design of VLSI Circuits (PC-3-1-0-4)	Elective-I (Professional) (PE-3-0-0-3)	Elective-II (Professional) (PE-3-0-0-3)	Elective-III (Professional) (PE-3-0-0-3)	18AEP21 Mini Project (PR-0-0-4-2)		23
III	Elective-IV (Professional) (PE-3-0-0-3)	Elective-V (Professional) (PE-3-0-0-3)	Elective-VI (Professional) (PE-3-0-0-3)	-	-	-	18AEP31 Project Work - Phase I (PR-0-0-12-6)		15
IV	-	-	-	-	-	-	18AEP41 Project Work – Phase II (PR-0-0-24-12)		12

Total Credits: 72

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M.E. DEGREE IN APPLIED ELECTRONICS

CURRICULUM

(For the candidates admitted from academic year 2018-19 onwards)

SEMESTER – I

Course Code	Course Title	Hours / Week			Credit	Maximum Marks			CBS
		L	T	P		CA	ESE	Total	
	Theory/Theory with Practical								
18AMT14	Advanced Mathematics for Electrical Engineers	3	1	0	4	50	50	100	HS
18PET11	System Theory	3	1	0	4	50	50	100	PC
18AET11	Modern Digital Signal Processing	3	1	0	4	50	50	100	PC
18AET12	CMOS VLSI Design	3	0	0	3	50	50	100	PC
18AET13	Computational Intelligence Techniques	3	0	0	3	50	50	100	PC
18AEC11	Embedded Systems	3	0	2	4	50	50	100	PC
	Total				**22**				

CA – Continuous Assessment, ESE – End Semester Examination, CBS – Curriculum Breakdown Structure

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M.E. DEGREE IN APPLIED ELECTRONICS

CURRICULUM

(For the candidates admitted from academic year 2018-19 onwards)

SEMESTER – II

Course Code	Course Title	Hours / Week			Credit	Maximum Marks			CBS
		L	T	P		CA	ESE	Total	
	Theory/Theory with Practical								
18AEC21	Design of Analog Integrated Circuits	3	0	2	4	50	50	100	PC
18AEC22	Digital System Design	3	0	2	4	50	50	100	PC
18VLE03	Low Power VLSI Design	3	1	0	4	50	50	100	PC
	Elective - I	3	0	0	3	50	50	100	PE
	Elective - II	3	0	0	3	50	50	100	PE
	Elective - III	3	0	0	3	50	50	100	PE
	Practical								
18AEP21	Mini Project	0	0	4	2	100	0	100	PR
	Total				**23**				

CA – Continuous Assessment, ESE – End Semester Examination, CBS – Curriculum Breakdown Structure

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M.E. DEGREE IN APPLIED ELECTRONICS

CURRICULUM

(For the candidates admitted from academic year 2018-19 onwards)

SEMESTER – III

Course Code	Course Title	Hours / Week			Credit	Maximum Marks			CBS
		L	T	P		CA	ESE	Total	
	Theory/Theory with Practical								
	Elective - IV	3	0	0	3	50	50	100	PE
	Elective - V	3	0	0	3	50	50	100	PE
	Elective - VI	3	0	0	3	50	50	100	PE
	Practical								
18AEP31	Project Work Phase I	0	0	12	6	50	50	100	PR
	Total				**15**				

CA – Continuous Assessment, ESE – End Semester Examination, CBS – Curriculum Breakdown Structure

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M.E. DEGREE IN APPLIED ELECTRONICS

CURRICULUM

(For the candidates admitted from academic year 2018-19 onwards)

SEMESTER – IV

Course Code	Course Title	Hours / Week			Credit	Maximum Marks			CBS
		L	T	P		CA	ESE	Total	
	Practical								
18AEP41	Project Work Phase II	0	0	24	12	50	50	100	PR
	Total				**12**				

CA – Continuous Assessment, ESE – End Semester Examination, CBS – Curriculum Breakdown Structure

Total Credits: 72

LIST OF PROFESSIONAL ELECTIVES						
Course Code	**Course Title**	**Hours/Week**			**Credit**	**CBS**
		L	**T**	**P**		
SEMESTER II						
18PEE02	Optimal Control Theory	3	1	0	4	PE
18VLT21	VLSI Signal Processing	3	0	0	3	PE
18COE04	Electromagnetic Interference and Compatibility	3	0	0	3	PE
18AEE01	Data Communication Networks	3	0	0	3	PE
18AEE02	Non-Conventional Energy Systems	3	0	0	3	PE
18AEE03	Programmable Logic Controllers	3	0	0	3	PE
18AEE04	Bio-Medical Signal Processing	3	0	0	3	PE
18AEE05	High Performance Communication Networks	3	0	0	3	PE
18AEE06	Programmable Digital Signal Processors	2	0	2	3	PE
SEMESTER III						
18MTE13	MEMS Design	3	0	0	3	PE
18COE13	Digital Image Processing and Multi Resolution Analysis	3	0	0	3	PE
18VLT12	Device Modeling	3	0	0	3	PE
18MSE18	Design and Analysis of Algorithms	3	0	0	3	PE
18MSE19	Internet Technologies	3	0	0	3	PE
18CIE15	Virtual Instrumentation for Industrial Applications	3	0	0	3	PE
18AEE07	Energy Conservation, Management and Auditing	3	0	0	3	PE
18AEE08	Project Management	3	0	0	3	PE
18AEE09	Wavelet Transforms and its Application	3	0	0	3	PE
18AEE10	SCADA and DCS	3	0	0	3	PE
18AEE11	Industrial Electronics	3	0	0	3	PE

18AMT14 ADVANCED MATHEMATICS FOR ELECTRICAL ENGINEERS

(Common to Applied Electronics & Power Electronics and Drives Branches)

L	T	P	Credit
3	1	0	4

Preamble	This course will help the students to identify, formulate and solve problems in electrical engineering using mathematical tools from a variety of mathematical areas, including matrix theory, calculus of variations, queuing theory and linear programming
Prerequisites	Calculus and Probability

UNIT – I **9**

Advanced Matrix Theory: Matrix factorizations – LU decomposition – The Cholesky decomposition – QR factorization – Least squares method – Generalized inverses – Singular value decomposition – Toeplitz matrices and Circulant matrices.

UNIT – II **9**

Calculus of Variations: Concept of variation – Euler equation – Variational problems with fixed boundaries – Variational problems involving several unknown functions – Functional involving first and second order derivatives – Functional involving several independent variables – Isoperimetric problems – Direct methods – Ritz method – Kantorowich method.

UNIT – III **9**

Stochastic Process: Definition – Classification of Stochastic Processes – Markov Chain -Transition Probability Matrices – Chapman Kolmogorov Equations - Classification of States – Continuous Time Markov Chains – Poisson Process - Birth and Death Processes.

UNIT – IV **9**

Queuing Models: Markovian queues – Single and Multi-server Models – Little's formula – Machine Interference Model - Non- Markovian Queues – Pollaczek Khintchine Formula.

UNIT – V **9**

Linear Programming: Formulation – Graphical solution – Simplex method – Big M method - Two phase method –Transportation and Assignment Problems.

Lecture:45, Tutorial:15, Total: 60

REFERENCES:

1. Richard Bronson, "Matrix Operations", 2nd Edition, Schaum's Outline Series, McGraw Hill, 2011.
2. Gupta A.S., "Calculus of Variations with Applications", 12th Edition, Prentice Hall of India Pvt. Ltd., New Delhi, 2015.
3. Roy D. Yates and David J. Goodman, "Probability and Stochastic Processes – A friendly Introduction for Electrical and Computer Engineers", John Wiley & Sons, 2005.
4. Taha H.A., "Operations Research: An Introduction", 10th Edition, Pearson Education, New Delhi, 2016.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	apply matrix computations in signal processing	Applying (K3)
CO2:	solve variational problems that occur in electrical engineering discipline	Evaluating (K5)
CO3:	use discrete time Markov chains to model computer systems	Applying (K3)
CO4:	exposing the basic characteristic features of a queuing system and acquire skills in analyzing queuing models	Applying (K3)
CO5:	develop a fundamental understanding of linear programming models	Evaluating (K5)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3
CO1	2		
CO2	2		
CO3	1		
CO4	1		
CO5	2		

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

18PET11 SYSTEM THEORY

(Common to Power Electronics and Drives & Applied Electronics branches)

L	T	P	Credit
3	1	0	4

Preamble	The aim of the subject is to give an adequate exposure to Z-Plane, State Space, Stability analysis and State Feedback Control
Prerequisites	Control Systems

UNIT – I **9**

Introduction to Digital Control System: Elements of Digital control system - Classifications of discrete time signals - Time domain models for discrete time systems. Sampling and reconstruction of signals - Frequency domain representation of sampling theorem - Nyquist rate, Aliasing. Mathematical model of sample and hold circuits-Practical aspects of choice of sampling rate.

UNIT – II **9**

Z-Plane Analysis of Discrete-Time Control Systems: Review of Z transform - Relationship between s plane and z plane - Difference equation representation of discrete time system - Pulse transfer function - Modified Z transform - Digital PID controllers - Zeigler - Nichols tuning method.

UNIT – III **9**

State Space Analysis and its Solution: Review of state space representation - Conversion of continuous state model to discrete state model - State diagram - Solution of discrete time state model: autonomous, non-autonomous systems - State transition matrix - Controllability and Observability - Multi variable discrete systems.

UNIT – IV **9**

State Feedback Control: Design of state feedback controller - Design of reduced and full order observers - Steady state error in state space - PI feedback - Digital compensator design - Digital filter properties - Kalman‟s filter.

UNIT – V **9**

Stability Analysis: BIBO stability - Effect of sampling rate on stability - Jury's stability test - Root Locus analysis - Asymptotic stability - Liapunov Stability Analysis of discrete time systems: Linear and Non-linear systems - Direct, Indirect method - Construction of Liapunov energy function.

Lecture: 45, Tutorial: 15, Total: 60

REFERENCES:

1. Gopal M., “Digital Control and State Variable Methods”, 4th Edition, Tata McGraw Hill, New Delhi, 2012.
2. Kuo B.C., “Digital Control Systems”, 2nd Edition, Oxford University Press, 2012.
3. Ogata K., “Discrete Time Control Systems”, 2nd Edition, Prentice Hall, New Jersey, 2011.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	explain the basic concepts in digital control system	Understanding (K2)
CO2:	analyze the discrete time control system by using Z-plane	Applying (K3)
CO3:	develop the mathematical model of linear discrete-time control systems using transfer functions and state-space models	Understanding (K2)
CO4:	analyze transient and steady-state behaviors of linear discrete-time control systems	Applying (K3)
CO5:	design controllers for linear discrete-time control systems as per the design criteria	Applying (K3)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3
CO1	3		2
CO2	2		3
CO3	2		2
CO4	2		3
CO5	2	2	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

18AET11 MODERN DIGITAL SIGNAL PROCESSING

L	T	P	Credit
3	1	0	4

Preamble	To introduce the fundamental concepts, principles and applications of Random signal, Multirate and Sparse signal processing techniques.
Prerequisites	Digital Signal Processing

UNIT – I **9**

Discrete Random Signal Processing: Discrete time random process - Random process: Ensemble averages- Gaussian process – Stationary process - The auto covariance and autocorrelation matrices – White noise - power spectrum. Parseval's theorem -Wiener Khintchine relation- Filtering random process - Spectral factorization.

UNIT – II **9**

Filters: The FIR Wiener filter - Filtering - Linear prediction - IIR Wiener Filter - Non causal IIR Wiener filter - Causal IIR Wiener filter. Adaptive Filter: Concepts of adaptive filter - FIR adaptive filter - LMS algorithm

UNIT – III **9**

Multirate Digital Signal Processing: Mathematical description of sampling rate - Interpolation and Decimation by integer factor - Sampling rate conversion by rational factor - Filter design for sampling rate conversion - Direct form FIR structures - Polyphase structures - Multistage implementation of sampling rate conversion.

UNIT – IV **9**

Uniform and Two Channel Filter Banks and Applications of DSP: Digital Filter Banks - Two-channel Quadrature Mirror Filter Bank - M-Channel QMF Bank. Applications: Noise cancellation using adaptive filtering technique - Sub band coding of speech signals - Design of decimation and interpolation filters.

UNIT – V **9**

Sparse Signal Processing: Sparse Signal Representation - Introduction - Sparse signals - Compressible signal - Over complete dictionaries - Coherence between the bases - Compressed sensing and signal reconstruction - Sensing in the presence of noise - Restricted isometry property.

Lecture:45, Tutorial:15, Total: 60

REFERENCES:

1. Hayes Monson H., "Statistical Digital Signal processing and Modeling", John Wiley & Sons Inc., 1996.
2. Proakis John G., and Manolakis Dimitris G., "Digital Signal Processing: Principles Algorithms and Applications", PHI, 2006.
3. Ifeachor Emmanuel C., and Jervis Barrie N., "Digital Signal Processing: A Practical Approach", Addison-Wesley Publishing Company, 2002.
4. Dionitris G. Manolakis, Vinay K. Ingle, Stepen M. Kogon, "Statistical and Adaptive Signal Processing, Spectral Estimation, Signal Modeling, Adaptive Filtering and Array Processing", McGraw-Hill International Edition, 2000.
5. Soman K.P., and Ramanathan R., "Digital Signal and Image Processing - The Sparse Way", Elseveir Publisher, 2012.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	illustrate the concepts and principles of random signal processing	Understanding (K2)
CO2:	design various filters for noise removal	Applying (K3)
CO3:	describe the concepts and principles of multirate digital signal processing	Understanding (K2)
CO4:	explain the concepts and principles of two channel, multichannel filter banks and design decimation and interpolation filters for real time application	Applying (K3)
CO5:	illustrate the concepts and principles of spare signal processing	Understanding (K2)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3
CO1	3		2
CO2	3		2
CO3	3		2
CO4	3		1
CO5	2		1

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

18AET12 CMOS VLSI DESIGN

L	T	P	Credit
3	0	0	3

Preamble	To understand the basic concepts of CMOS VLSI circuits using logic design, physical structure and fabrication of semiconductor devices and to build systems for efficient VLSI data processing.
Prerequisites	VLSI Design

UNIT – I **9**

VLSI Design Process and Basic CMOS: VLSI Design Process – Types of ASICs – ASIC Design Flow – MOS Transistors – CMOS Logic – NMOS and PMOS transistors - Threshold voltage – Body effect – MOS Design equations – Second order effects – MOS models – CMOS inverter DC characteristics – Small signal AC characteristics.

UNIT – II **9**

CMOS Processing Technology: Silicon semiconductor technology – Wafer processing – Oxidation – Selective Diffusion – Silicon Gate Process. CMOS technology: Nwell – Pwell process – Twin tub process – Silicon on insulator – CMOS process enhancement – Stick Diagram – Layout Diagram – Layout design rules.

UNIT – III **9**

Circuit Characterization and Performance Estimation: Resistance estimation – Capacitance estimation – Switching characteristics – CMOS gate transistor sizing – Power Consumption– Charge sharing – Scaling of MOS transistors

UNIT – IV **9**

CMOS Logic Circuit Design: CMOS Logic Structures – CMOS Combinational Logic Circuits: Static CMOS Design – Dynamic CMOS design. CMOS Sequential Logic Circuits: Timing Metrices – Static Latches and Registers – Dynamic Latches and Registers

UNIT – V **9**

CMOS Subsystem Design: Adders – Binary Counters – Multipliers – Data Path circuits – Static and Dynamic RAM cell Design – ROM cells – PLA Design.

Total: 45

REFERENCES:

1. Neil H.E. Weste, "CMOS VLSI Design: A Circuits and Systems Perspective" (For VTU), 3rd Edition, Pearson Education, 2012.
2. Albert Raj A., and Latha T., "VLSI Design", 3rd Edition, PHI Learning Pvt. Ltd., 2011.
3. Smith M.J.S., "Application Specific Integrated Circuits", Pearson Education, 1997.
4. Wolf Wayne, "Modern VLSI Design–System on chip Design", 3rd Edition, Prentice Hall Inc., 2002.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	understand VLSI design flow and CMOS transistor characteristics	Understanding (K2)
CO2:	explain different fabrication technologies for CMOS transistors	Understanding (K2)
CO3:	estimate the various CMOS circuit parameters	Applying (K3)
CO4:	construct various logic structures in CMOS circuits	Applying (K3)
CO5:	examine various CMOS subsystems	Analyzing (K4)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3
CO1	2	1	3
CO2	2	1	2
CO3	3	1	3
CO4	3		2
CO5	2	1	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

18AET13 COMPUTATIONAL INTELLIGENCE TECHNIQUES

(Common to Applied Electronics & Power Electronics and Drives Branches)

L	T	P	Credit
3	0	0	3

Preamble	This course serves as a guide to explore computer methodology and algorithms that improves automatically through experience.
Prerequisites	Numerical methods

UNIT – I **9**

Artificial Neural Networks: Introduction to Soft computing – Neural Networks – Model – activation functions – architecture – Supervised learning – Perceptrons – Adaline and Madaline – Back propagation algorithm – Radial Basis Function Networks – Unsupervised Learning and Other Neural Networks – Competitive Learning Networks – Kohonen Self Organizing Networks – Learning Vector Quantization – Hebbian Learning.

UNIT – II **9**

Fuzzy Logic: Fuzzy Sets – Basic Definition and Terminology – Set theoretic operations – Membership function formulation and parameterization - Extension principle and Fuzzy Relations- Fuzzy if-then Rules – Fuzzy Reasoning – Fuzzy Inference Systems – Mamdani Fuzzy Models –Sugeno Fuzzy Models –Tsukamoto Fuzzy Models – Input Space Partitioning - Fuzzy Modeling.

UNIT – III **9**

Optimization Techniques: Derivative based Optimization: Descent Methods –The Method of steepest Descent – Classical Newton's Method – Step Size Determination – Derivative free Optimization: Genetic Algorithms – Simulated Annealing – Particle swarm Optimization - Ant colony optimization.

UNIT – IV **9**

Neuro Fuzzy Modeling: Adaptive Neuro Fuzzy Inference Systems – Architecture – Hybrid learning Algorithm –learning methods that Cross-fertilize ANFIS and RBFN – Coactive Neuro fuzzy Modeling – Framework – Neuron Functions for Adaptive Networks – Neuro Fuzzy spectrum.

UNIT – V **9**

Applications: Printed Character Recognition – Inverse kinematics Problem – Applications of soft computing techniques for power electronics: MPPT - Speed control for electrical machines - Harmonic elimination techniques in power converters.

Total: 45

REFERENCES:

1. Jang J.S.R., Sun C.T., and Mizutani E., "Neuro-Fuzzy and Soft Computing", PHI, Pearson Education, 2004.
2. Laurene V. Fausett, "Fundamentals of Neural Networks: Architectures, Algorithms and Applications", 3rd Edition, Pearson Education, 2008.
3. Timothy J. Ross, "Fuzzy Logic with Engineering Applications", Wiley India.
4. David E. Goldberg, "Genetic Algorithms: Search, Optimization and Machine Learning", Addison Wesley, New York, 1989.
5. Bimal K. Bose, "Neural Network Applications in Power Electronics and Motor Drives-An Introduction and Perspective", IEEE Transactions on Industrial Electronics, Vol.54, Issue: 1, pp.14-33,February 2007.
6. Whei-Min Lin, Chih-Ming Hong and Chiung-Hsing Chen, "Neural Network Based MPPT Control of a Stand Alone Hybrid Power Generation System", IEEE Transactions on Power Electronics, Vol.26, Issue: 12, pp.3571 – 3581, December 2011.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	interpret and analyze various artificial neural networks	Understanding (K2)
CO2:	examine the concepts of fuzzy systems	Analyzing (K4)
CO3:	gain fundamental knowledge on optimization techniques and its implementation procedures	Understanding (K2)
CO4:	illustrate various hybrid topology of neuro fuzzy system	Understanding (K2)
CO5:	develop suitable soft computing technique on real time systems	Applying (K3)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3
CO1	2	1	2
CO2	3		2
CO3	3		2
CO4	2	1	3
CO5	3		2

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

18AEC11 EMBEDDED SYSTEMS

L	T	P	Credit
3	0	2	4

Preamble	To comprehend the microcontroller family and its programming concepts for designing and controlling a real time embedded system. Further, this course is aimed at imparting the various concepts of Real time operating system.
Prerequisites	Microprocessors and Microcontrollers

UNIT – I **9**

Introduction: Introduction to Embedded systems – Von Neumann and Harvard architecture – Need of Microcontrollers – selection criterion. PIC Microcontroller 16F87X: Architecture – Features – Resets –Memory Organisations: Program Memory, Data Memory – Instruction Set – Simple programs using Assembly language Instruction sets – Interrupts.

UNIT – II **9**

Physical Interface Support Using PIC: PIC Peripherals – I/O Parallel Ports – Timers – Capture/Compare/PWM (CCP) Modules - Control registers – Serial ports – Master Synchronous serial Port (MSSP) in I^2C mode and in SPI mode – USART – Interfacing of PIC: Analog-to-digital Converter (ADC) – Registers associated with the peripherals – Initializing the Peripheral modules using Assembly language.

UNIT – III **9**

Arm Processor And Programming: General concepts - ARM7 - Instruction Set Architecture, Levels in architecture, Functional description - processor and memory organization - Introduction to RISC architecture, pipelining, Instruction issue and execution - Instruction formats - Addressing modes - Data alignment and byte ordering – Simple programs using Assembly language Instruction sets.

UNIT – IV **9**

Embedded Programming: Programming in Assembly Language (ALP) Vs High level language – C Program elements, Macros and Functions – Use of pointers – NULL pointers – use of function calls – Multiple function calls in a cyclic order in the main function pointers – Function queues and interrupt Service Routines queues - pointers. C program compilers – Cross compiler – optimization of memory codes.

UNIT – V **9**

Real-Time Operating Systems and Design: Introduction - RTOS Necessity - Operating system services –I/O subsystems – Network operating systems –Interrupt Routines in RTOS Environment – RTOS Task scheduling models – IEEE standard POSIX functions for standardization of RTOS and inter-task communication functions - Fifteen point strategy for synchronization between processors, ISRs, OS Functions and Tasks – OS security issues - Embedded system design and Co-Design Issues in System Development process – Design cycle in the development phase for an embedded system –Issues in Embedded System Design.

List of Exercises / Experiments :

1. Study of PIC16F8X Microcontroller kit.
2. ALP for arithmetic operations using PIC16F87X.
3. ALP for I/O port access using PIC16F87X.
4. C programming Serial for I/O port access using PIC16F87X.
5. C programming for Parallel I/O port access using PIC16F87X.

6.	C programming for Display Interfacing using PIC16F87X.
7.	C programming for Rolling Display Interfacing using PIC16F87X.
8.	C programming for Timer/RTC Interfacing using PIC16F87X.
9.	C programming for Memory Interfacing using PIC16F87X.
10.	C programming for Stepper Motor Interfacing using PIC16F87X.

Lecture:45, Practical:30, Total: 75

REFERENCES:

1.	Ajay V. Deshmukh, "Microcontrollers: Theory and Applications", Tata McGraw Hill, New Delhi, 2007.
2.	Raj Kamal, "Embedded Systems Architecture, Programming and Design", Tata McGraw-Hill, New Delhi, 2007.
3.	Wayne Wolf, "Computers as Components: Principles of Embedded Computing System Design", 2nd Edition, Morgan Kaufman Publishers, San Francisco, 2001.
4.	Vahid Frank and Givargi Tony, "Embedded System Design: A Unified Hardware/Software Introductions", John Wiley & Sons, New York, 2001.
5.	Packages: MPLAB IDE, WINXTALK, PICC Compiler

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	illustrate the basic architecture and demonstrate the interfacing concepts of PIC16 microcontroller	Understanding (K2)
CO2:	apply the programming skills for peripheral interfacing and real time applications	Applying (K3)
CO3:	illustrate the basic architecture and demonstrate the interfacing concepts of ARM processor	Understanding (K2)
CO4:	develop, analyze and demonstrate the use of embedded C programming concepts	Understanding (K2)
CO5:	apply the concepts of RTOS and real-time systems design techniques to various software programs	Applying (K3)
CO6:	develop the assembly language program to perform arithmetic operations and I/O data transfer applications	Applying (K3), Articulation (S4)
CO7:	make use of the C programming concepts for performing serial and parallel I/O communications.	Applying (K3), Manipulation (S2)
CO8:	build C programming for interfacing memory, timing and display devices and apply the techniques for controlling the Stepper motor	Applying (K3), Manipulation (S2)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3
CO1	3		2
CO2	3		2
CO3	3		3
CO4	3		3
CO5	3		2
CO6	3		2
CO7	3		2
CO8	3		2

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

18AEC21 DESIGN OF ANALOG INTEGRATED CIRCUITS

L	T	P	Credit
3	0	2	4

Preamble	To inculcate the design knowledge of analog integrated circuits in terms of modeling and configuring amplifiers, filters, multipliers, and data converters.
Prerequisites	Electronic Circuits

UNIT – I **9**

Integrated Circuits, Device Models and Measurement of Model Parameters: Introduction to Analog Device Design – Depletion region of a PN junction- DC, Small Signal and High Frequency Model for Diode, BJT and MOS Transistor - Measurement of Model Parameters - Switches, Active resistors**.**

UNIT – II **9**

Circuit Configuration of IC and Current Sources and Sinks, Current Mirrors: Circuit configuration of IC- Simple,Wilson, Cascade current sources, Voltages and Current References-Band gap voltage references.

UNIT – III **9**

Basic Analog Amplifiers and Differential Amplifiers: MOS inverting amplifier, improving the performance of inverting amplifier - CMOS Differential amplifiers - Characteristics of Operational amplifiers Types: Two stage CMOS- Cascade- Folded cascade- Transconductance amplifiers.

UNIT – IV **9**

Filters, Comparators, Multipliers and Mixed Signal IC: Lowpass filters, High pass filters, Band pass filters, Switched Capacitor filters,comparators, and multipliers - Introduction to mixed signal IC.

UNIT – V **9**

Data Converters: Data Converter fundamentals, DAC Architectures: Current Switched, Resistive, Charge redistribution, Hybrid, Segmented D/A Converters. ADC architectures: Flash, Integrating, Successive Approximation and folding A/D Converters. Over sampling Converters.

Lecture :45, Practical:30, Total: 75

List of Exercises / Experiments :

1. Simulation of Current Mirror and DesignPCB layout using ORCAD
2. Simulation of Wein Bridge Oscillators and DesignPCB layout using ORCAD
3. Simulation of a differential amplifier circuit and Design PCB layout using ORCAD
4. Simulation of filter circuit using MATLAB\ORCAD
5. Simulation\Implementation of data converters using MATLAB\ORCAD

REFERENCES / MANUALS / SOFTWARES:

1. Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, Robert G. Meyer, "Analysis and Design of Analog Integrated Circuits", 5th Edition , John Wiley & Sons, New York, 2001.
2. Allen Phillips E., and Holberg Douglas R., "CMOS Analog Circuit Design", 2nd Edition, Oxford University Press, Oxford, 2003.
3. Johns David A., and Martin Ken, "Analog Integrated Circuit Design", John Wiley & Sons, NewYork, 2002.
4. Randall L. Geiger, Phillips E. Allen, Noel R. Strader, "VLSI Design Techniques for Analog and Digital Circuits", McGraw Hill International Editions, 1990.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	explain the concepts of device models and its parameters	Understanding (K2)
CO2:	analyze transistor current mirrors and voltage & current references	Applying (K3)
CO3:	comprehend basic analog and differential Amplifiers	Applying (K3)
CO4:	demonstrate filters, comparators and multipliers	Applying (K3)
CO5:	determine the architecture of data converters	Applying (K3)
CO6:	develop current mirror and differential amplifier circuit and simulate using software	Applying (K3), Manipulation (S2)
CO7:	build and assess the performance of oscillator and simulate using software	Evaluating (K5), Manipulation (S2)
CO8:	implement and test filter, data converters and simulate using software	Applying (K3), Manipulation (S2)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3
CO1	3		2
CO2	3		2
CO3	3	1	2
CO4	2		3
CO5	2		3
CO6		3	
CO7		3	2
CO8			3

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

18AEC22 DIGITAL SYSTEM DESIGN

L	T	P	Credit
3	0	2	4

Preamble	To design a complete digital system and implement using various FPGA processors. Further, this course is aimed at analyzing and diagnosing various faults involved in the digital system.
Prerequisites	Digital Logic Circuits, VLSI Systems

UNIT – I **9**

Advanced Topic in Sequential Logic Design: ASM Chart – ASM Realization for Synchronous Logic circuit –Analysis of Asynchronous Sequential Circuit (ASC) – Flow Table Reduction – Races in ASC – State Assignment – Problem and the Transition Table – Design of ASC – Static and Dynamic Hazards – Essential Hazards.

UNIT – II **9**

System Design Using VHDL: VHDL Description of Combinational Circuits – Arrays – VHDL Operators – Compilation and Simulation of VHDL Code – Modeling using VHDL – Flip Flops –Registers - Counters – Sequential Machine – Combinational Logic Circuits – VHDL Code for Serial Adder, Binary Multiplier – Binary Divider .

UNIT – III **9**

Field Programmable Gate Arrays: Types of FPGA – XILINX XC3000 series – Logic Cell Array (LCA) – Configurable Logic Blocks (CLB) – Input/Output Blocks (IOB) – Programmable Interconnection Points (PIP) – XILINX XC4000 Series –Introduction to Xilinx SPARTAN-6, VIRTEX-5 FPGA.

UNIT – IV **9**

Introduction to Zynq Processor and Fault Modeling: Case Study Xilinx Zynq, Zynq APU, ZynqSoC Design Overview, Zynq Architecture and Design Flow, Device Selection Criteria, Zynq versus FPGA, Zynq versus Standard Processor, Zynq versus Dicrete FPGA Processor. Introduction to Testing – Faults in digital circuits – Modeling of faults – Logical Fault Models – Fault detection – Fault location – Fault dominance.

UNIT – V **9**

Fault Diagnosis and Testability Algorithms: Fault Table Method – Path Sensitization Method-Boolean Difference Method – D Algorithm – Tolerance Techniques – Fault in PLA – DFT – Test Generation –Built-in Self Test.

List of Experiments:

1. Design and Simulation of digital circuits using VHDL.
2. Design and Simulation of digital circuits using Verilog.
3. FPGA Implementation of combinational and sequential logic circuit.
4. Implementation of signal and image processing HDL design using VIVADO.
5. Zynq Board: Implement Timers and GPIO modules in FPGA and control it with ARM SOC.
6. Design of Dynamic latches using SPICE.
7. Design and Simulation of Dynamic CMOS circuits using SPICE.

Lecture :45, Practical:30, Total: 75

REFERENCES:

1. Roth Jr. Charles H. LizyKurian John, “Digital System Design Using VHDL”, 2nd Edition, Cengage Learning Publication, 2012.
2. Michael L. Bushnell, Vishwani D. Agrawal, “Essentials of Electronic Testing for Digital Memory and Mixed Signal VLSI Circuits”, Kluwer Academic Publications, USA, 2002.
3. Nripendra N. Biswas, “Logic Design Theory”, Prentice Hall of India, 2001.
4. Parag K. Lala, “An Introduction to Logic Circuit Testing”, Morgan and Claypool Publishers, 2009.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	design and analyze asynchronous sequential circuits	Creating (K6)
CO2:	write VHDL code for various digital logic circuits	Applying (K3)
CO3:	explain the architecture and features of FPGA families	Understanding (K2)
CO4:	test and analyze the various faults in logic circuits	Understanding (K2)
CO5:	identify and diagnose the faults in logic circuits	Applying (K3)
CO6:	design a combinational and sequential logic circuit	Applying (K3), Articulation (S4)
CO7:	simulate VHDL code for various digital logic circuits	Applying (K3), Precision (S3)
CO8:	implement various digital logic circuits using FPGA boards	Applying (K3), Manipulation (S3)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3
CO1	3	1	3
CO2	3	2	2
CO3	2	1	2
CO4	3	1	3
CO5	3	1	3
CO6	3	1	3
CO7	3	2	2
CO8	2	1	2

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

18VLE03 LOW POWER VLSI DESIGN

(Common to VLSI Design and Applied Electronics branches)

L	T	P	Credit
3	1	0	4

Preamble	To design the combinational and sequential circuits with minimum power consumption and to anlayse the various power optimization methods and techniques to reduce power consumption.
Prerequisites	VLSI Design Techniques

UNIT – I **9**

Power dissipation in CMOS: Hierarchy of limits of power – Sources of power consumption – Physics of power dissipation in CMOS FET devices – Basic principle of low power design

UNIT – II **9**

Power Optimization: Logic level power optimization – Circuit level low power design – circuit techniques for reducing power consumption in adders and multipliers.

UNIT – III **9**

Design of Low Power CMOS Circuits: Computer arithmetic techniques for low power system – reducing power consumption in memories – low power clock, Inter connect and layout design – Advanced techniques –Special techniques.

UNIT – IV **9**

Power Estimation: Power Estimation techniques – logic power estimation – Simulation power analysis – Probabilistic power analysis.

UNIT – V **9**

Software Design for Low Power: Sources of Software Power dissipation - Power Estimation - Power Optimization - Automated low power code generation - Codesign for low power.

Lecture:45, Tutorial: 15, Total: 60

REFERENCES:

1. Kaushik Roy and Prasad S.C., "Low Power CMOS VLSI Circuit Design", Reprint, Wiley, 2014.
2. Dimitrios Soudris, Chirstian Pignet, Costas Goutis, "Designing CMOS Circuits for Low Power", 4th Edition, Kluwer, Springer, 2010.
3. Kulo J.B. and Lou J.H., "Low Voltage CMOS VLSI Circuits", Wiley, 1999.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	enumerate the different sources of power dissipation in CMOS	Understanding (K2)
CO2:	analyze various power optimization technique at circuit level	Analyzing (K4)
CO3:	design of low power circuits at architecture level	Creating (K6)
CO4:	use of simulation and probabilistic method of power analysis	Analyzing (K4)
CO5:	perform power estimation and optimization at programming level	Evaluating (K5)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3
CO1	3		2
CO2	2		3
CO3	3	1	3
CO4	1		1
CO5	3	1	2

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

18PEE02 OPTIMAL CONTROL THEORY

(Common to Power Electronics and Drives & Applied Electronics branches)

L	T	P	Credit
3	1	0	4

Preamble	The objective of the course is to build and analyze models for time varying systems and non linear systems
Prerequisites	System Theory

UNIT – I **9**

Introduction: Review - Models for Time-varying and Nonlinear systems, state space representation, matrix theory, static optimization with and without constraints. Calculus of variations-basic concepts- functional of a single function and several functions - necessary conditions and boundary conditions.

UNIT – II **9**

Optimal Control Formulation: Performance measures for optimal control problems-Hamiltonian approach-necessary conditions for optimal control- Linear regulator problem-infinite time regulator problem-, Regulators with a prescribed degree of stability.

UNIT – III **9**

The Minimum (Maximum) Principle: Pontryagin‘s minimum principle and state inequality constraints, Minimum time problem, Minimum control energy problems. Singular intervals in optimal control.

UNIT – IV **9**

Numerical Techniques: Numerical solution of two-point boundary value problem –Gradient method and Quasi Linearisation method - solution of Ricatti equation by iterative method.

UNIT – V **9**

Dynamic Programming: Principle of optimality - recurrence relation of dynamic programming for optimal control problem - computational procedure for solving optimal control problems - characteristics of dynamic programming solution - dynamic programming application to discrete and continuous systems - Hamilton Jacobi Bellman equation. Relationship between Dynamic Programming and Minimum Principle.

Lecture:45, Tutorial:15,Total: 60

REFERENCES:

1. Kirk Donald, “Optimal Control Theory”, Prentice Hall, New Jersey,1970.
2. Anderson B.D.O. and Moore J.B., “Optimal Control: Linear Quadratic Methods”, Prentice Hall, New Jersey, 1979.
3. Desineni Subburam Naidu, “Optimal Control Systems”, CRC Press, 2003.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	analyze models for time varying systems and non linear systems	Applying (K3)
CO2:	apply the optimal control functions to solve the stability related problems	Applying (K3)
CO3:	analyze the problems using minimum (maximum) principles and numerical techniques	Analyzing (K4)
CO4:	design controllers using various numerical techniques	Analyzing (K4)
CO5:	explain the concept of dynamic programming to solve optimal control problems	Understanding (K2)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3
CO1	2	1	2
CO2	2	1	2
CO3	2	1	2
CO4	3	1	2
CO5	3	1	2

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

18VLT21 VLSI SIGNAL PROCESSING

(Common to VLSI Design and Applied Electronics branches)

L	T	P	Credit
3	0	0	3

Preamble	To apply the concepts of VLSI techniques to real time signal processing
Prerequisites	Digital Signal Processing

UNIT – I **9**

Introduction to DSP Systems: Introduction To DSP Systems -Typical DSP algorithms. **Iteration Bound** – data flow graph representations, loop bound and iteration bound, Algorithms For Computing Iteration Bound, Iteration Bound of Multirate Data Flow Graphs. **Pipelining and Parallel Processing:** Pipelining of FIR digital filters, parallel processing, pipelining and parallel processing for low power.

UNIT – II **9**

Retiming: Definitions and properties retiming techniques; solving systems of inequalities, retiming techniques. **Unfolding:** Algorithm for unfolding, properties of unfolding, critical path unfolding and retiming applications of unfolding- sample period reduction and parallel processing application.

UNIT – III **9**

Systolic Architecture Design: Design methodology, FIR systolic arrays. **Bit Level Arithmetic Architectures:** Parallel Multipliers, Bit-Serial Multipliers, Bit-Serial Filter Design and Implementation, Canonic Signed Digit Arithmetic, Distributed Arithmetic.

UNIT – IV **9**

Fast Convolution: Fast convolution – Cook-Toom algorithm, modified Cook-Took algorithm – Wino grad Algorithm, Modified Wino grad Algorithm. **Algorithmic Strength Reduction:** Algorithmic strength reduction in Filters-Parallel FIR Filters, DCT and Inverse DCT. **Pipelined and Parallel Recursive filters Adaptive Filters:** Pipelining in first- order IIR filters, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.

UNIT – V **9**

Scaling, Round off Noise: Scaling and Round off Noise- State variable Description of digital filters, Scaling and round off noise computation, Round off noise in pipelined I order IIR filters. **Lattice Structure:** Introduction, Schur algorithm, Digital basic Lattice Filters, Derivation of One-Multiplier Lattice Filter, Derivation of Normalized Lattice filter. **Numerical Strength Reduction:** Introduction, Sub expression Elimination, Multiple Constant Multiplication, Sub expression Sharing in Digital Filters, Additive and Multiplicative Number Splitting.

Total: 45

REFERENCES:

1. Parhi K. Keshab, "VLSI Digital Signal Processing Systems, Design and Implementation", Reprint, John Wiley, Inter Science, New York, 2008.
2. Isamail, Mohammed and Fiez, Terri, "Analog VLSI Signal and Information Processing", McGraw-Hill, New York, 2007.
3. www.pdf-search-engine.com/vlsi-signal-processing-pdf.html

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	compute the iteration bound of a circuit	Applying (K3)
CO2:	perform pipelining and parallel processing in FIR systems to achieve high speed and low power	Applying (K3)
CO3:	improve the speed of digital system through transformation techniques	Applying (K3)
CO4:	apply systolic and bit level architectures to improve the efficiency of VLSI circuits	Applying (K3)
CO5:	use of proper techniques for parallel processing design for scaling and roundoff noise computation	Applying (K3)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3
CO1	1		1
CO2	3	1	2
CO3	3	1	3
CO4	3		2
CO5	2		2

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

18COE04 ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY

(Common to Communication Systems,VLSI Design, Applied Electronics & Power Electronics and Drives branches)

L	T	P	Credit
3	0	0	3

Preamble	To expose the basics and fundamentals of Electromagnetic Interference and Compatibility in Communication System Design and to know the concepts of EMI Coupling Principles, EMI Measurements and Control techniques and the methodologies of EMI based PCB design.
Prerequisites	Electromagnetic Principles

UNIT – I **9**

EMI Environment: EMI/EMC concepts and definitions, Sources of EMI, conducted and radiated EMI, Transient EMI, Time domain Vs Frequency domain EMI, Units of measurement parameters, Emission and immunity concepts, ESD.

UNIT – II **9**

EMI Coupling Principles: Conducted, Radiated and Transient Coupling, Common Impedance Ground Coupling, Radiated Common Mode and Ground Loop Coupling, Radiated Differential Mode Coupling, Near Field Cable to Cable Coupling, Power Mains and Power Supply coupling.

UNIT – III **9**

EMI/EMC Standards and Measurements: Civilian standards - FCC, CISPR,I EC, EN, Military standards - MIL STD 461D/462, EMI Test Instruments /Systems, EMI Shielded Chamber, Open Area Test Site, TEM Cell, Sensors/Injectors/Couplers, Test beds for ESD and EFT, Military Test Method and Procedures (462).

UNIT – IV **9**

EMI Control Techniques: EMI Control Techniques : Shielding, Filtering, Grounding, Bonding, Isolation Transformer, Transient Suppressors, Cable Routing, Signal Control, Component Selection and Mounting

UNIT – V **9**

EMC Design of PCBs: PCB Traces Cross Talk, Impedance Control, Power Distribution Decoupling, Zoning, Motherboard Designs and Propagation Delay Performance Models.

Total: 45

REFERENCES:

1. Ott W. Henry, "Noise Reduction Techniques in Electronic Systems", 2nd Edition, John Wiley & Sons, New York, 2008.
2. Kodali V.P., "Engineering EMC Principles, Measurements and Technologies", 2nd Edition, IEEE Press, London, 2006.
3. Keiser Bernhard, "Principles of Electromagnetic Compatibility", 3rd Edition, Artech House, Dedham, 1987.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	estimate the EMI and analyze in time domain and frequency domain	Analyzing (K4)
CO2:	compare the various EMI coupling methods	Evaluating (K5)
CO3:	conduct the EMI measurement for civilian and military appliances	Analyzing (K4)
CO4:	device the EMI control techniques	Applying (K3)
CO5:	evaluate the PCB'S and motherboards EMI performance and design the EMC circuits	Creating (K6)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3
CO1	1		
CO2	2	1	
CO3	3	3	
CO4		1	2
CO5	2	2	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

18AEE01 DATA COMMUNICATION NETWORKS

(Common to Applied Electronics & Power Electronics and Drives branches)

L	T	P	Credit
3	0	0	3

Preamble	To provide understanding of the concepts of computer networks, multiple access techniques, network protocols, the upper layers of the OSI model, internetworking and emerging trends in networking technologies
Prerequisites	Nil

UNIT – I **9**

Introduction: Definition of Networks–Classification of Networks–LAN, MAN, WAN, internet–Network Topology – Protocols and Standards – Network Models – OSI, TCP/IP Models of networking – Internet.

UNIT – II **9**

Physical Layer: Review of Signals–Data Rate Limits–Performance Issues–Bandwidth,Throughput, Latency, Bandwidth-Delay Product, Jitter. Digital Transmission and Analog Transmission: Line coding techniques, PCM and Delta Modulation techniques – ASK, FSK, PSK, and QAM Techniques – Bandwidth Utilization: Multiplexing and Spreading.

UNIT – III **9**

Communication Media and Data Link Layer: Data Transmission using Telephone Networks–Dial-up MODEMS, Digital Subscriber Line (DSL).Error Detection and Correction techniques:Linear and Cyclic codes–Data Link Control: Framing, Flow and Error Control – HDLC and PPP protocols. Multiple Access Techniques – CSMA, CSMA/CD, CSMA/CA – Channelization – TDMA, FDMA, and CDMA.

UNIT – IV **9**

Wired LANs and WANs: Wired LANs–IEEE 802 standards - Ethernet–IEEE 802.3 MAC Frame–Token RingLAN - IEEE 802.5 MAC Frame – Wireless LANs – IEEE 802.11 standard – Bluetooth Technology – Interconnection of LANs. Wired WANs - Circuit-Switched Networks, Datagram Networks, Virtual Circuit- switched Networks, Structure of Circuit and Packet Switches - Wireless WANs.

UNIT – V **9**

Internetworking: Internetworking–tunneling–IP Addressing Scheme–Structure of IP Datagram–IP Routing – TCP as Transport Layer Protocol – Structure of TCP Segment – TCP Connection: Establishment and Closing – SMTP Protocol for E- Mail Application.

Total: 45

REFERENCES:

1. Forouzan Behrouz A., "Data Communications and Networking", 4th Edition, Tata McGraw-Hill, New Delhi, 2006.
2. Peterson Larry L. and Davie Bruce S., "Computer Networks: A Systems Approach", 4th Edition, Elsevier Publications, New Delhi, 2007.
3. Rowe Stanford H. and Schuh Marsha L., "Computer Networking", Pearson Education, New Delhi, 2005.
4. Kurose James and Ross Keith, "Computer Networking: Top Down Approach featuring the Internet", Pearson Education, New Delhi, 2002.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	explain the basic concepts of networking	Understanding (K2)
CO2:	acquire the knowledge of various performance parameters and modulation techniques	Understanding (K2)
CO3:	schedule the network components and the functioning of data link layer	Applying (K3)
CO4:	classify various IEEE standards of wireless networks	Applying (K3)
CO5:	manipulate the addressing scheme and summarize the operations of TCP/IP	Applying (K3)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3
CO1	1	2	1
CO2	1	2	
CO3	1		
CO4		1	
CO5	1	1	1

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

18AEE02 NON-CONVENTIONAL ENERGY SYSTEMS					
		L	**T**	**P**	**Credit**
		3	**0**	**0**	**3**
Preamble	To make the student familiar with the Energy Scenario, Renewable Energy Sources, Power Production and its conversion.				
Prerequisites	Nil				
UNIT-I					**9**
Introduction: Energy Conservation and Energy Efficiency – Needs and Advantages, Different types of Renewable Energy Sources - Availability of Energy Resources in World –Environmental aspects of energy utilization – Energy Conservation Act 2001 - Statistical Report on Renewable energy scenario in India - Distributed generations.					
UNIT-II					**9**
Solar Energy and its Power Converters: Introduction to solar energy: Solar radiation, availability, measurement and estimation – Solar thermal conversion devices and storage – solar energy collectors - Solar heating and cooling techniques – Solar desalination – Solar Pond – Solar cooker – Solar Drying – Solar pumping– solar cells and photovoltaic conversion – PV systems – MPPT. Applications of PV Systems.					
UNIT-III					**9**
Wind Energy and its Power Converters: Introduction – Basic principles of wind energy conversion – wind data and energy estimation – site selection consideration – basic components of wind energy conversion system –Types of wind machines – basic components of wind electric conversion systems. Schemes for electric generations – generator control, load control, energy storage – applications of wind energy – Inter connected systems.					
UNIT-IV					**9**
Geothermal and Biomass Energy: Introduction, estimation of geothermal power, nature of geothermal fields, geothermal sources, inter connection of geothermal fossil systems, prime movers for geo thermal energy conversion. Application of geothermal energy. Energy from biomass: Introduction, Biomass conversion technologies, photosynthesis, classification of biogas plants. Biomass Energy conversion, Energy from waste.					
UNIT-V					**9**
Chemical Energy Sources: Introduction – fuel cells – design and principles of operation of a fuel cell – classification of fuel cells. Types of fuel cells – conversion efficiency of fuel cells. Types of electrodes, work output and EMF of fuel cell, Applications of fuel cells. Hydrogen energy: Introduction – hydrogen production – electrolysis, thermo chemical methods, Westing House Electro-chemical thermal sulphur cycle. Fossil fuel methods. Hydrogen storage, Utilization of hydrogen gas.					
					Total: 45

REFERENCES:

1. Sukatme S.P., "Solar Energy – Principles of Thermal Collection and Storage", 2nd Edition, Tata McGraw Hill, 2008.
2. Rai G.D., "Non Conventional Energy Sources", Khanna Publishes, 1993.
3. Efstathios E (Stathis) Michaelides, "Alternate Energy Sources", Springer Science and Business Media, 2012.
4. Goswami D.Y., Kreith F. and Kreider J.F., "Principles of Solar Engineering", 2nd Edition, CRC Press, 2000.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	conceptualize the Energy Scenario around the World and in India	Understanding (K2)
CO2:	understand the Solar Energy Generation and its Power Conversion	Understanding (K2)
CO3:	determine Wind Energy Production and its Converters	Applying (K3)
CO4:	employ Geothermal and Biomass Energy	Applying (K3)
CO5:	demonstrate Fuel cell and Hydrogen Energy Production	Applying (K3)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3
CO1	2		2
CO2	2		2
CO3	3		2
CO4	3	1	2
CO5	2		2

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

18AEE03 PROGRAMMABLE LOGIC CONTROLLERS

(Common to Applied Electronics & Power Electronics and Drives branches)

L	T	P	Credit
3	0	0	3

Preamble	The aim of the subject is to develop an understanding of the basic concepts of PLC, advanced PLC programming, installation &troubleshooting and to develop industrial applications.
Prerequisites	Nil

UNIT – I **9**

Introduction to Programmable Logic Controller: Overview of Programmable Logic Controller - Architecture – Principle of operation - I/O Modules: Discrete, Analog, Special – I/O Specifications – CPU – Memory design and types – Programming devices – Recording and Retrieving data –PLC programming languages.

UNIT – II **9**

Basic PLC Programming: Fundamentals of Logic – Program Scan– Relay-Type Instructions - Instruction addressing – Branch and Internal relay instructions – Entering the Ladder diagram – Electromagnetic Control relays – Contactors – Motor Starters – Manual operated switches and Mechanically operated switches.

UNIT – III **9**

Advanced PLC Programming: Programming Timers – Programming Counters – Program Control Instructions – Data Manipulation Instructions – Math Instructions – Sequencer and Shift Register Instructions.

UNIT – IV **9**

PLC Installation and Troubleshooting: PLC Enclosures – Electrical Noise – Leaky Inputs and Outputs – Grounding – Voltage Variations and Surges – Program Editing – Programming and Monitoring – Preventive Maintenance – Connecting PC and PLC.

UNIT – V **9**

PLC Communication and its Applications: Computer Fundamentals – Computer-Integrated Manufacturing – Data Communications – Computer numeric control – Robotics - PLC Applications: Bottle filling system – Pneumatic stamping system – Material handling system – Spray Painting system– Traffic light control system.

Total: 45

REFERENCES:

1. Frank D. Petruzella, “Programmable Logic Controllers” , Tata McGraw-Hill Edition, New Delhi, 2010.
2. Webb John W. and Reis Ronald A., “Programmable Logic Controllers”, Prentice Hall Publications, New Delhi, 2005.
3. Bolton W., “Programmable Logic Controllers”, Elsevier, New York, 2006.
4. Rockwell Automation, “Logix 5000 Controllers” – system reference

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	identify the PLC hardware and programming languages for various applications	Applying (K3)
CO2:	develop PLC ladder logic programming for industrial problems	Applying (K3)
CO3:	design a PLC system, component, or process to meet a set of specifications	Applying (K3)
CO4:	install and troubleshoot the PLC	Analyzing (K4)
CO5:	apply the PLC in various industrial applications	Applying (K3)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3
CO1	2	1	2
CO2	3	1	3
CO3	3	1	3
CO4	3		3
CO5	3		3

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

18AEE04 BIO-MEDICAL SIGNAL PROCESSING				
	L	**T**	**P**	**Credit**
	3	**0**	**0**	**3**
Preamble	To analyze various bio-medical signals and apply different signal processing techniques on bio signals for classification and compression.			
Prerequisites	Digital Signal Processing			
UNIT – I				**9**
Biomedical Signals, Filtering and Modeling: Nature of Biomedical signals, Types: Action, Potential,Electroneurogram(ENG),Electromyogram(EMG),Electrocardiogram(ECG), Electroencephalogram (EEG), Event related potentials, Electrogastrogram (EGG), Phonocardiogram (PCG), Speech signals				
UNIT – II				**9**
Stationary versus Non-stationary Processes: Time domain filters, Frequency domain filters, Optional filters, Adaptive filters for removal of Interference, Selection of Appropriate filters, Applications. Parametric System modeling, Autoregressive or All-pole modeling, Pole-zero modeling, Electromechanical Models of Signal Generation, Application: Heart-rate variability – Spectral modeling and Analysis of ECG signals				
UNIT – III				**9**
Non-stationary Signals, Classification and Decision: EEG rhythms and waves, characterization of non stationary signals and dynamic systems, Fixed segmentation, Adaptive segmentation.				
UNIT – IV				**9**
Pattern Classification and Compression Techniques: Supervised, Unsupervised Pattern classification, Probabilistic models and Statistical Decision, Regression analysis-Compression and Advanced Topics: Direct Digital compression Techniques, Transformation Compression Techniques, Other Compression Techniques and Comparison.				
UNIT – V				**9**
Introduction to Wavelet Transforms: Application of Wavelet Transform on Biomedical Signals, Multi Resolution Analysis. Neural Networks in Processing and Analysis of Bio medical Signals.				
				Total: 45

REFERENCES:

1.	Rangaraj M. Rangayyan, "Biomedical Signal Analysis, A case study Approach", IEEE Press, 2001.
2.	Bronzino Joseph D., "The Biomedical Engineering Handbook", 3rd Edition, Taylor and Francis, 2006.
3.	Reddy D.C., "Biomedical Signal Processing, Principles and Techniques", Tata McGraw Hill, New Delhi, 2005.
4.	Banner Kenneth E. and Arce Gonzalo R., "Nonlinear Signal and Image Processing: Theory Methods and Applications", CRC Press, New York, 2003.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	explain the various bio medical signals	Understanding (K2)
CO2:	design different types of filters for various biomedical applications	Applying (K3)
CO3:	differentiate stationary and non-stationary signal processing	Understanding (K2)
CO4:	describe the pattern classification and compression techniques on bio signals	Applying (K3)
CO5:	apply wavelet transform and neural network concepts to analyze biomedical signals	Analyzing (K4)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3
CO1	2		2
CO2	3		3
CO3	3	1	2
CO4	3	1	2
CO5	3		3

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

18AEE05 HIGH PERFORMANCE COMMUNICATION NETWORKS				
	L	**T**	**P**	**Credit**
	3	**0**	**0**	**3**

Preamble	High performance communication networks deals with fundamentals of Packet switched networks and the architectures, functions, performance of different communication networks. In this course, features and performance of ATM, Advanced Network architecture, Bluetooth technology and various protocols are to be discussed.
Prerequisites	Nil

UNIT – I	**9**
Packed Switched Networks: OSI and IP Models, Ethernet,(IEEE 802.3), Token (IEEE 802.5) Wireless LAN (IEEE 802.11) FDDI,DQDB,SMDS: Internet Working with SMDS.	

UNIT – II	**9**
ISDN and broadband ISDN: ISDN Overview, Interfaces and Functions, layers and Services- Signalling Systems, Broadband ISDN- Architecture and Protocols	

UNIT – III	**9**
ATM and Frame Relay: ATM - Main Features- Addressing, Signaling and Routing, ATM Header structure-Adaptation Layer, Management and Control, ATM Switching and Transmission. Frame Relay: Protocols and Services, Congestion Control ,Internet working with ATM, Internet and ATM, Frame relay via ATM.	

UNIT – IV	**9**
Advanced Network Architecture: IP forwarding architectures overlay model – Multi Protocol Label Switching (MPLS) – Integrated services in the Internet – Resource Reservation Protocol (RSVP) – Differentiated services	

UNIT -V	**9**
Blue Tooth Technology: The Blue tooth module – Protocol stack Part I: Antennas – Radio interface – Base band – The Link controller – Audio – The Link Manager – The Host controller interface -The Blue tooth module – Protocol stack Part I: Logical link control and adaptation protocol – RFCOMM – Service discovery protocol – Wireless access protocol – Telephony control protocol	

Total: 45

REFERENCES:

1.	Jean Walrand and Pravinvaraiya, "High Performance Communication Networks", 2nd Edition, Harcourt and Morgan Kauffman, London, 2000.
2.	William Stallings, "ISDN and Broadband ISDN with Frame Relay and ATM", 4th Edition, Pearson Education Asia, 2002.
3.	Kasera Pankaj Sethi, "ATM Networks", Tata McGraw-Hill, New Delhi, 2000.
4.	Jennifer Bray and Charles F. Sturmen, "Bluetooth", Pearson Education, Asia, 2001.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	explain the architectures and mechanisms of high-performance communication networks	Understanding (K2)
CO2:	apply the concepts of ISDN and BISDN protocols to communication networks	Applying (K3)
CO3:	analyze the cause of congestion, traffic slow down, Quality of Service and features of ATM and frame relay	Analyzing (K4)
CO4:	inspect the features of advanced communication network analysis,design of service, availability, and security	Analyzing (K4)
CO5:	examine the features of Bluetooth technology and its protocols	Analyzing (K4)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3
CO1	3	1	2
CO2	3		3
CO3	2	1	2
CO4	3	1	2
CO5	3		3

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

18AEE06 PROGRAMMABLE DIGITAL SIGNAL PROCESSORS

(Common to Applied Electronics & Power Electronics and Drives branches)

L	T	P	Credit
2	0	2	3

Preamble	This course brings the DSP processors architecture, addressing modes and programming with DSP processors. It also provides an insight to the various types of on-chip peripherals, interfacing methods and various applications.
Prerequisites	Digital Signal Processing, Microprocessors and Microcontrollers

UNIT – I **6**

Architectures of Programmable Digital Signal Processors: Introduction, Basic Architectural Features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Features for External Interfacing.

UNIT – II **6**

TMS320C5416 Digital Signal Processor: TMS320C5416: Introduction: History Development and Advantages of TMS320 DSPs, Applications. TMS320C5416: Functional Overview Features, Architectural Overview, Pin configuration, Registers, Addressing modes, On-Chip Peripherals, Memory Map, Instruction set. Simple Programs: Addition, Multiplication, Division, Convolution. Introduction to Code Composer studio.

UNIT – III **6**

Interfacing peripherals with TMS320C5416: I/O Interface, ADC Interface, DAC Interface, CODEC Interface. Program: Switch and LED Interfacing, Square wave generation, Saw tooth wave generation**.**

UNIT – IV **6**

TMF28335 Digital Signal Processor: TMF28335 DSP: Overview, Key features: Hardware Features, Software Features, Architecture, Pin configuration, Memory Map, Switches: Boot Load option switch, Processor configuration switch, Power Connector.

UNIT – V **6**

Interfacing peripherals with TMF28334: I/O Interface, ADC Interface, DAC Interface, PWM Module. Programs: Switch and LED interfacing, ADC Port Control, PWM generation.

List of Exercises / Experiments :

1. Generation and Convolution of signals using MATLAB
2. Square Wave form Generation using TMS320C5416 Digital Signal Processor
3. Saw tooth waveform Generation using TMS320C5416 Digital Signal Processor
4. Variable PWM waveform generation using TMF28335 Digital Signal Processor
5. Switch and LED Interfacing using TMF28335 Digital Signal Processor

Lecture:30, Practical:30, Total:60

REFERENCES:

1. Avatar Singh, Srinivasan S., "Digital Signal Processing- Implementation using DSP Microprocessors with Examples from TMS320C54xx", Thomson India, 2004.
2. Venkataramani B. and Bhaskar M., "Digital Signal Processors, Architecture, Programming and Applications", 2nd Edition, Tata Mc Graw Hill, 2010.
3. User Manual: VSK5416 & eZdspTMF28335 Technical Reference

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	explain the Basic architectural features of DSP processors	Understanding (K2)
CO2:	describe the various features and programming concepts of TMS320C5416 DSP	Understanding (K2)
CO3:	apply the Interfacing mechanism to interface various peripherals with TMS 320C5416 DSP	Applying (K3)
CO4:	point out the functionality of TMSF28355 DSP	Understanding (K2)
CO5:	employ the Interfacing mechanism of various peripherals with TMS 320C5416 DSP and its programming concepts.	Applying (K3)
CO6:	make use of modern software tool to generate various form of signals	Applying (K3), Manipulation (S2)
CO7:	apply embedded c program for generating waveforms using DSP320C5416	Applying (K3), Manipulation (S2)
CO8:	demonstrate the PWM waveform Generation and I/O interfacing using DSPF28355	Applying (K3), Precision (S3)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3
CO1	2	1	
CO2	2	1	
CO3	3	2	1
CO4	2	1	
CO5	3	1	1
CO6	3	1	1
CO7	3	1	1
CO8	3	1	1

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

18MTE13 MEMS DESIGN

(Common to Mechatronics, CADCAM, Engineering Design, VLSI Design, Applied Electronics, Power Electronics and Drives & Control and Instrumentation Engineering branches)

L	T	P	Credit
3	0	0	3

Preamble: This course equips the students to understand the concepts of Micro mechatronics and apply the knowledge of micro fabrication techniques for various applications.

Prerequisites: Sensors and Instrumentation and Bridge course mechanical

UNIT – I **9**

Materials for MEMS and Scaling Laws: Overview - Microsystems and microelectronics - Working principle of Microsystems - Si as a substrate material - Mechanical properties - Silicon compounds - Silicon piezo resistors - Gallium arsenide - Quartz-piezoelectric crystals - Polymer - Scaling laws in Miniaturization.

UNIT – II **9**

Micro Sensors, Micro Actuators: Micro sensors - Micro actuation techniques - Micro actuators – Micromotors – Microvalves – Micro grippers – Micro accelerometer: introduction, types, actuating principles, design rules, modeling and simulation, verification and testing, applications.

UNIT – III **9**

Mechanics for Microsystem Design: Static bending of thin plates - Mechanical vibration - Thermo mechanics - Thermal stresses - Fracture mechanics - Stress intensity factors, fracture toughness and interfacial fracture mechanics-Thin film Mechanics-Overview of Finite Element Stress Analysis.

UNIT – IV **9**

Fabrication Process and Micromachining: Photolithography - Ion implantation - Diffusion – Oxidation – CVD - Physical vapor deposition - Deposition by epitaxy - Etching process- Bulk Micro manufacturing - Surface micro machining – LIGA –SLIGA.

UNIT – V **9**

Micro System Design, Packaging and Applications: Design considerations - Process design - Mechanical design – Mechanical Design using Finite Element Method-Micro system packaging – Die level - Device level - System level – Packaging techniques - Die preparation - Surface bonding - Wire bonding – Sealing - Applications of micro system in Automotive industry: Bio medical, Aerospace and Telecommunications – CAD tools to design a MEMS device.

Total: 45

REFERENCES:

1. Tai-Ran Hsu, "MEMS and Microsystems Design and Manufacture", Tata McGraw-Hill, New Delhi, 2008.
2. Mohamed Gad-el-Hak, "The MEMS Handbook", CRC Press, 2009.
3. Bao M.H., "Micromechanical Transducers: Pressure sensors, accelrometers, and gyroscopes", Elsevier, New York, 2000.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	interpret the concepts of MEMS materials and scaling laws	Remembering (K1)
CO2:	explain the principles of micro sensors and actuators	Understanding (K2)
CO3:	apply the mechanics for micro system design	Applying (K3)
CO4:	design and fabrication of microsystem	Applying (K3)
CO5:	design of microsystem packaging and application	Applying (K3)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3
CO1	2	1	2
CO2	2	1	2
CO3	3	1	3
CO4	3	1	3
CO5	3	1	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy BT - Blooms Taxonomy

18COE13 DIGITAL IMAGE PROCESSING AND MULTI RESOLUTION ANALYSIS

(Common to Communication Systems, Mechatronics, Information Technology & Applied Electronics branches)

L	T	P	Credit
3	0	0	3

Preamble	To analyze the images in frequency domain and to perform various operations like enhancement, Restoration, Compression, Registration and Multi resolution analysis.
Prerequisites	Digital Signal Processing

UNIT – I **9**

Image Transforms: Orthogonal transforms – FT, DST, DCT, Hartley, Walsh hadamard, Haar, Radon, Slant Wavelet, KL, SVD and their properties.

UNIT – II **9**

Image Enhancement and Restoration: Image enhancement - Point operations - contrast stretching - clipping and thresholding - digital negative intensity level slicing - bit extraction. Histogram processing - histogram equalisation -modification. Spatial operations – smoothing spatial filters, sharpening spatial filters. Transform operations. Color image enhancement. Image Restoration – degradation model, Noise models, Unconstrained and Constrained restoration, Inverse filtering – removal of blur caused by uniform linear motion, Wiener filtering, Restoration by SVD and Homomorphic filtering

UNIT – III **9**

Image Compression: Image Compression – Need for data compression – Run length encoding – Huffman coding – Arithmetic coding – predictive coding- transform based compression, - vector quantization – block truncation coding. Image Segmentation: Point, Edge and line detection -thresholding-Region based approach Image Representation: boundary based – region based and intensity based description

UNIT – IV **9**

Registration and Multivalued Image Processing: Registration – geometric transformation – registration by mutual information Mutivalued image processing – colour image processing – colour image enhancement-satellite image processing- radiometric correction – other errors- multi spectral image enhancement- medical image processing – image fusion.

UNIT – V **9**

Wavelets and Multiresolution Processing: Image Pyramids – Subband coding – The Haar Transform – Multiresolution Expansion – Series Expansion – Scaling Function – Wavelet Function – Wavelet Transform in One Dimension- The Wavelet Series Expansion – The Discrete Wavelet Transform – The Continuous Wavelet Transform – The Fast Wavelet Transform – Wavelet transform in two dimensions– Applications in image denoising and compression.

Total: 45

REFERENCES:

1. Gonzalez Rafel C. and Woods Richard E., "Digital Image Processing", 4th Edition, Prentice Hall, New York, 2017.
2. Chanda B., Dutta Majumder D., "Digital Image Processing and Analysis", 2nd Edition, PHI Learning, 2011.
3. Abdeljalil Ouahabi, "Signal and Image Multiresolution Analysis", John Wiley & Sons, 2012.
4. Rosenfield Azriel and Kak Avinash C., "Digital Picture Processing", 2nd Edition, Academic Press Inc., New York, 1982.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	implement the image enhancement and image restoration techniques	Applying (K3)
CO2:	model the systems to enhance and restore the image optimally	Applying (K3)
CO3:	apply the coding technique to perform compression of images	Applying (K3
CO4:	apply the concepts of registration to fuse images of various modalities	Applying (K3)
CO5:	analyze the images in one dimension and two dimension simultaneously	Analyzing (K4)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3
CO1	3	2	1
CO2	3	2	1
CO3	3	2	1
CO4	3	2	1
CO5	2	3	2

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy BT - Blooms Taxonomy

18VLT12 DEVICE MODELING

(Common to VLSI Design & Applied Electronics branches)

L	T	P	Credit
3	0	0	3

Preamble	To model and analyze the performance of solid state devices using mathematical concepts
Prerequisites	Solid State Devices

UNIT – I **9**

Semiconductor Physics and Modeling of Passive Devices: Quantum Mechanical Concepts - Carrier Concentration - Transport Equation - Mobility and Resistivity - Carrier diffusion - Carrier Generation and Recombination - Continuity equation - Tunneling and High field effects - Modeling of resistors - Modeling of Capacitors - Modeling of Inductors.

UNIT – II **9**

Diode and Bipolar Device Modeling: Abrupt and linear graded PN junction - Ideal diode current equation - Static, Small signal and Large signal models of PN junction Diode - SPICE model for a Diode - Temperature and Area effects on Diode Model Parameters Transistor Action - Terminal currents – Switching - Static, Small signal and Large signal Eber-Moll models of BJT - Temperature and area effects.

UNIT – III **9**

MOSFET Modeling and Parameter Measurements: MOS Transistor - NMOS - PMOS - MOS Device equations - Threshold Voltage - Second order effects - Temperature Short Channel and Narrow Width Effect - Models for MOSFET.

UNIT – IV **9**

Noise Models and BSIM4 MOSFET Model: Noise Sources in MOSFET - Flicker Noise Modeling - Thermal Noise Modeling - BSIM4 MOSFET Model - Gate Dielectric Model - Enhanced Models for Effective DC and AC Channel Length and width - Threshold Voltage Model-I-V Model.

UNIT – V **9**

Other MOSFET Models: EKV Model - Model Features - Long Channel Drain Current Model - Modeling Second order Effects of Drain Current - Effect of Charge Sharing - Modeling of Charge storage Effects - Non-quasi static Modeling - Noise Models - Temperature Effects - MOS Model 9-MOSAI Model

Total: 45

REFERENCES:

1. Trond Ytterdal, Yuhua Cheng and Tor A. Fjeldly, "Device Modeling for Analog and RF CMOS Circuit Design", John Wiley & Sons Ltd., 2003.
2. Sze S.M., "Semiconductor Devices - Physics and Technology", 2nd Edition, John Wiley & Sons, New York, 2008.
3. Massobrio Giuseppe and Antognetti Paolo, "Semiconductor Device Modeling with SPICE", 2nd Edition, McGraw-Hill Inc., New York, 1998.
4. Tyagi M.S., "Intorduction to Semiconductor Materials and Devices", John Wiley, New York, 2003.
5. Ben G. Streetman, "Solid State Circuits", 5th Edition, Prentice Hall of India, New Delhi, 2005.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	realize the concepts of semiconductor physics	Understanding (K2)
CO2:	apply mathematical concepts to model basic semiconductor devices	Applying (K3)
CO3:	analyze the secondary effects of semiconductor physics using mathematical expressions	Analyzing (K4)
CO4:	analyze the effects of temperature and Area on the performance of semiconductor devices	Analyzing (K4)
CO5:	create models for MOSFETs	Creating (K6)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3
CO1	2	2	2
CO2	2	1	1
CO3	3	3	3
CO4	2	2	2
CO5	2	1	1

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy BT - Blooms Taxonomy

18MSE18 DESIGN AND ANALYSIS OF ALGORITHMS

(Common to Embedded Systems & Applied Electronics branches)

L	T	P	Credit
3	0	0	3

Preamble: To introduce the fundamental concepts of designing strategies, complexity analysis of algorithms, followed by problems on graph theory and sorting methods and also includes the basic concepts on complexity theory.

Prerequisites: C and Data Structures

UNIT – I **9**

Introduction: The Role of Algorithms in Computing – Growth of Functions – Analysis of Recursive and Non-recursive Functions – Lists – Heap Sort – Quick Sort – Sorting in Linear Time.

UNIT – II **9**

Advanced Data Structures: Binary Search Trees – Red-Black Trees – Augmenting Data Structures – Trees – Fibonacci Heaps

UNIT – III **9**

Algorithm Design Techniques: Dynamic Programming – Rod cutting – Matrix-chain multiplication – Elements of dynamic programming – Longest common subsequence – Optimal binary search trees. Greedy Algorithms: An activity-selection problem – Elements of the greedy strategy – Huffman codes – Matroids and greedy methods – A task-scheduling problem as a matroid Parallel Algorithms**:** Parallelism Introduction – The Pram Model – Simple parallel operations – Parallel searching, sorting, numerical algorithms – Parallel Graph algorithms

UNIT – IV **9**

Graph Algorithms: Elementary Graph Algorithms – Minimum Spanning Trees – Single Source Shortest Paths – All-Pairs Shortest Paths – Maximum Flow.

UNIT – V **9**

Non-Deterministic Algorithms: NP-Completeness: Polynomial Time verification – NP Completeness and Reducibility – NP Completeness Proofs – NP Complete Problems

Total: 45

REFERENCES:

1. Thomas H. Cormen, Charles E. Leiserson, Ronald L. Rivest and Clifford Stein, "Introduction to Algorithms", 3rd Edition, MIT Press, USA, 2009.
2. Jeffrey J. McConnell Canisius College, "Analysis of Algorithms: An Active Learning Approach", Jones and Bartlett Publishers, 2001.
3. Aho Alfred V., Hopcroft John E. and Ulllman Jeffrey D., "Data Structures and Algorithms", Pearson Education, New Delhi, 2002.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	design and implement elementary data structures	Creating (K6)
CO2:	design and implement advanced data structures	Creating (K6)
CO3:	choose appropriate algorithm design technique and solve problems	Applying (K3)
CO4:	implement graph algorithms	Applying (K3)
CO5:	analyze the time and space complexity of algorithms	Analyzing (K4)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3
CO1	1	2	
CO2		2	
CO3	2		
CO4	3	1	
CO5	2	2	

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

18MSE19 INTERNET TECHNOLOGIES

L	T	P	Credit
3	0	0	3

Preamble: This course covers the basic concept of internet and network applications

Prerequisites: Nil

UNIT-I **9**

Introduction to Internet: Internet-network edge - network core - access networks & physical media – NAPs, ISPs and Internet backbones- delay & loss in packet-switched networks- protocol layers & their service models

UNIT-II **9**

Network Applications: Principles of Network applications- Application layer protocols: World Wide Web Architecture, HTTP and its working principle, File Transfer Protocol, e-mail components and SMTP, Internet directory service DNS-Streaming Audio and Video – Internet Radio- VoIP-Content Delivery.

UNIT-III **9**

Transport and Network Layers: Transport layer services and principles - multiplexing and demultiplexing applications -connectionless transport: UDP - principles of reliable data transfer – TCP connection establishment and termination- Introduction & network service models –Virtual circuit and datagram networks-– Internet Protocol (IP)- forwarding and addressing- Fragmentation and reassembly – IPv6.

UNIT-IV **9**

WEB 2.0: Introduction-search-content networks- blogging- social networking-social media-tagging-social bookmarking-software development-Rich Internet Applications-Web services-location based services-XML-RSS- Atom-JSON-Monetization models-business models-Future of the web.

UNIT-V **9**

XHTML and Cascading Style Sheets: Introduction-Editing XHTML-W3C-Headings-Linking-Images-Lists-Tables-Forms-Internal Linking-meta elements-web resources-CSS-different categories of CSS-positioning elements-backgrounds-element dimensions-box model and text flow-media types-building CSS drop down menu-user style sheets.

Total: 45

REFERENCES:

1. Kurose K.F. and Ross K.W., "Computer Networking: A Top - Down Approach Featuring The Internet", 5th Edition, Pearson Education, New Delhi, 2009.
2. Tanenbaum Andrew S. "Computer Networks", 5th Edition, Pearson Education, New Delhi, 2010.
3. Deitel P.J. and Deitel H.M., "Internet & World Wide Web How to Program", 4th Edition, Pearson Education, New Delhi, 2009.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	summarize the basic concepts of internet	Understanding (K2)
CO2:	describe various applications of network	Understanding (K2)
CO3:	explain the transport and network layers with the services	Understanding (K2)
CO4:	build Internet application using WEB 2.0	Applying (K3)
CO5:	create web pages using cascading style sheets	Applying (K3)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3
CO1	1		
CO2	1		
CO3	1		
CO4	2		1
CO5	2		1

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

18CIE15 VIRTUAL INSTRUMENTATION FOR INDUSTRIAL APPLICATIONS

(Common to Control and Instrumentation Engineering, Embedded Systems, Applied Electronics & Power Electronics Drives branches)

L	T	P	Credit
3	0	0	3

Preamble	To impart knowledge about advanced tools in virtual instrumentation to develop new industrial applications
Prerequisites	Virtual Instrumentation

UNIT – I **9**

Graphical System Design Programming Concepts: G-Programming- debugging techniques-Loops: For loop, While Loop, Shift registers-Structures: Case Structure, Sequence Structure, Event Structure, Timed Structure-

UNIT – II **9**

Data Acquisition and Interfacing: Data Acquisition in LabVIEW-Hardware installation and configuration-DAQ components-DAQ signal Accessory-DAQ Assistant-DAQ Hardware-DAQ Software.

UNIT – III **9**

GSD Programming Toolkits: Signal Processing and Analysis-Control System Design and Simulation-Digital Filter Design-Spectral Measurements-Report generation-PID Control-Biomedical Startup kit.

UNIT – IV **9**

VI Applications Part I: Material Handling System -Fiber-Optic Component Inspection Using Integrated Vision and Motion Components-Internet-Ready Power Network Analyzer for Power Quality Measurements and Monitoring.

UNIT – V **9**

VI Applications Part II: Developing Remote Front Panel LabVIEW Applications- Using the Timed Loop to Write Multirate Applications in LabVIEW - Client–Server Applications in LabVIEW- Neural Networks for Measurement and Instrumentation in Virtual Environments.

Total: 45

REFERENCES:

1. Jovitha Jerome, "Virtual Instrumentation using LabVIEW", 3rd Edition, PHI Learning Pvt. Ltd., New Delhi, 2012.
2. Sumathi S., Surekha P., "LabVIEW based Advanced Instrumentation Systems", Springer Science & Business Media, 2007.
3. Sanjay Gupta, Joseph, John, "Virtual Instrumentation using LabVIEW", 2nd Edition, Tata McGraw Hill, 2010.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	apply structured programming concepts in developing VI programs and employ various debugging techniques	Applying (K3)
CO2:	interface hardware devices with software using DAQ system	Applying (K3)
CO3:	design, implement and analyze an application using different tools	Applying (K3)
CO4:	apply knowledge on various tools in practical works	Applying (K3)
CO5:	create virtual instruments for real time applications	Applying (K3)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3
CO1	1	1	1
CO2	2	1	2
CO3	2	2	2
CO4	2	2	1
CO5	2	2	2

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

18AEE07 ENERGY CONSERVATION, MANAGEMENT AND AUDITING

(Common to Applied Electronics & Power Electronics and Drives branches)

L	T	P	Credit
3	0	0	3

Preamble	The aim of the course is to understand the basics of energy conservation techniques, energy auditing in industries and the associated economical benefits.
Prerequisites	Nil

UNIT – I **9**

Energy: Energy Scenario – India and World – Energy Resources Availability in India– Energy consumption – Pattern, Energy and Environment - Energy Security - Energy Conservation and its importance, Energy Conservation Act, 2001 and its features

UNIT – II **9**

Energy Conservation in Thermal Systems: Energy Conservation in Thermal Systems – Needs and Advantages. – Properties of steam –Assessment of steam distribution losses, steam leakages, steam trapping, Various Energy Conservation measures in Steam Systems – Losses in Boilers, Energy Conservation opportunities in Boilers

UNIT – III **9**

Energy Management: Importance of Energy Management, Financial analysis Techniques – Simple Payback Period, Return on Investment, Net present Value, Internal Rate of Return, Cash flows, Risk and Sensitivity Analysis, Financing Options, Energy Performance Contract and Role of ESCOS.

UNIT – IV **9**

Energy Efficient technologies in Electrical System: Maximum Demand Controllers, Automatic Power Factor Controllers, Energy Efficient motors, Soft starters with Energy Saver, Variable speed drives, Energy Efficient transformers, Electronic Ballast, Energy Efficient Lighting Controls- Occupancy Sensors, Time based control.

UNIT – V **9**

Energy Audit: Energy Audit – Need, Principle, Types, Methodologies, Energy audit approach, Barriers, Role of Energy Manager and Auditor – Energy Audit Questionnaire – Bench marking and Energy Performance – Energy Audit Instruments, Case study.

Total: 45

REFERENCES:

1. "Book I - General Aspect of Energy Management and Energy Audit", 3rd Edition, Bureau of Energy Efficiency, Ministry of Power, India, 2010,
2. "Book II - Energy Efficiency in Thermal Utilities", 3rd Edition, Bureau of Energy Efficiency, Ministry of Power, India, 2010.
3. "Book III - Energy Efficiency in Electrical Utilities", 3rd Edition, Bureau of Energy Efficiency, Ministry of Power, India, 2010.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	outline the energy scenario	Understanding (K2)
CO2:	apply the energy performance measures in thermal system	Applying (K3)
CO3:	apply various financial techniques for economic analysis	Applying (K3)
CO4:	apply the energy performance measures in electrical system	Applying (K3)
CO5:	explain the principles and methodologies of energy audit	Understanding (K2)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3
CO1	2		1
CO2	3	1	3
CO3	3	1	2
CO4	3	1	3
CO5	2	2	2

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

18AEE08 PROJECT MANAGEMENT

(Common to Applied Electronics & Power Electronics and Drives branches)

L	T	P	Credit
3	0	0	3

Preamble	This course serves as a guide to learn and execute various phases of undertaking a project.
Prerequisites	Nil

UNIT – I **9**

Philosophy and Concepts: Need – Goals- Evolution-Different Forms -Project Management in Manufacturing, Service and Government Sectors; Systems Development Cycle – Conception phase: proposal, contracting – Definition phase – Execution phase: production / build, implementation – Operation phase- System Development in Industries, service and government sectors - case study.

UNIT – II **9**

Planning Fundamentals: Planning Steps – Project master plan - Tools for project planning – work break down structure, responsibility matrix, events and mile stones- Gantt charts. Network Scheduling – the critical path – early and late times – slack –float – calendar scheduling.

UNIT – III **9**

PERT: Time estimates – probability of finishing by target completion date – criticisms of PERT - CPM – Time cost relationship – reducing project duration – shortest duration – total project cost; Scheduling with Resource Constraints – resource loading and leveling – constrained resources; Introduction to GERT network - case studies in PERT/CPM.

UNIT – IV **9**

Project Cost Estimation: Process – classification-expert opinion, analogy estimate, parametric estimate, cost engineering, Contingency amount - Elements of budgets and Estimates – direct labour, direct non- labour, overhead, general and administrative expenses, profit and total billing. Project cost accounting – budgeting using cost accounts - cost summaries, cost schedules and forecasts – case study. Project Management Information Systems (PMIS): Functions – Computer based PMI Systems – Web-Based project management

UNIT – V **9**

Project Control: Cost accounting systems- project control process - Project control emphasis- Performance Analysis – cost, schedule, work package analysis, performance indices, updating time estimates, technical performance measurement- Performance Index monitoring – variance limits, controlling changes, contract administration, control problems, case study. Project Evaluation: Review meetings, reporting, terminating, termination responsibilities, closing the contract, project extensions, project summary evaluation.

Total: 45

REFERENCES:

1. Nicholas John M., "Project Management for Business and Technology", Prentice Hall India, New Delhi, 2011.
2. Pagnoni Anastasia, "Project Engineering: Computer Oriented Planning and Operational Decision Making", Springer-Verlag, Berlin, 2012.
3. Pannerselvam R., "Project Management", PHI Learning Pvt. Ltd., 2010.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	understanding of a schematic carrying out a project indicating various phases	Understanding (K2)
CO2:	apply project management techniques for executing projects	Applying (K3)
CO3:	understand various control measures in project implementation	Understanding (K2)
CO4:	analysis the techniques and procedures for defining, scheduling and budgeting project activities to achieve project quality, time, and cost goals.	Evaluating (K5)
CO5:	monitor, evaluate, control and executing the project.	Evaluating (K5)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3
CO1	3	1	2
CO2	3	1	2
CO3	3	2	2
CO4	3	2	2
CO5	3	2	2

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

18AEE09 WAVELET TRANSFORMS AND ITS APPLICATIONS

L	T	P	Credit
3	0	0	3

Preamble	To analyze the properties of different types of wavelet transform and its applications on image processing.
Prerequisites	Digital Signal Processing

UNIT - I **9**

Introduction: Vector spaces - properties - dot product - basis-dimension, orthogonality and orthonormality - relationship between vectors and signals-signal spaces-concept of convergence-Hilbert spaces for energy signals.

UNIT - II **9**

Fourier Analysis and STFT: Fourier Transform-drawbacks of Fourier analysis- window function - Short-time Fourier Transform (STFT) analysis-spectrogram plot-phase-space plot in time-frequency plane. Heisenberg's uncertainty principle-Tilling of the time-frequency plane for STFT.

UNIT - III **9**

Continuous Wavelet Transform: Wavelet transform properties-concept of scale and its relation with frequency-continuous Wavelet Transform (CWT)-scaling function and wavelet functions: Daubechies, Haar, Coiflet, Mexican hat, Sine, Gaussian, Bi-orthogonal wavelets - Tilling of time scale plane for CWT.

UNIT - IV **9**

Discrete Wavelet Transform and Multi-Resolution Analysis: Discrete Wavelet Transform (DWT)-Filter bank and sub-band coding principles. Multi-resolution analysis-Time scale difference equations for wavelets and scaling functions-Wavelet filters-scale variation in discrete domain-Mallet's algorithm for DWT-Inverse DWT computation by filter banks. Introduction to multiwavelet transforms.

UNIT - V **9**

Wavelet Packet Analysis and Applications: Haar wavelet packets–application–best basis selectionand cost functions. Sub-band coding of images-Image compression-Image de-noising – image coding using wavelet tree coder – EZW code and SPIHT code. Introduction to second generation wavelets.

Total: 45

REFERENCES:

1. Mallat S., "A Tour on Wavelet Signal Processing", Elsevier, New Delhi, December 2005.
2. Rao R.M. and Bopardikar A.S., "Wavelet Transforms", Addison Wesley, 1999.
3. Soman K.P. and Ramachandran K.I., "Insight into Wavelets-From Theory to Practice", Prentice Hall of India, New Delhi, 2010.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	explain the vector space and properties of signals	Understanding (K2)
CO2:	elaborate the Fourier transforms and its time frequency plane	Understanding (K2)
CO3:	analyze the various properties of wavelet transform and classify them	Analyzing (K4)
CO4:	describe the discrete wavelet transform and mutiresolution analysis	Understanding (K2)
CO5:	apply wavelet transform for various signal and image processing applications	Applying (K3)

Mapping of COs with Pos

COs/POs	PO1	PO2	PO3
CO1	2	1	2
CO2	3	1	2
CO3	2	1	2
CO4	3	1	2
CO5	3	1	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

18AEE10 SCADA AND DCS

(Common to Applied Electronics & Power Electronics and Drives branches)

L	T	P	Credit
3	0	0	3

Preamble	The aim of the subject is to develop an understanding of the basic concepts of automation system using SCADA & DCS and to develop the industrial applications using the same.
Prerequisites	Digital Logic Circuits

UNIT – I **9**

Automation: Fundamentals of industrial automation, need and role of automation, evolution of automation. HMI systems, Text display – operator panels – Touch panels – Panel PCs – Integrated displays (PLC and HMI), Rack installation, Grounding and shielding, physical, electrical, maintenance requirements- Troubleshooting.

UNIT – II **9**

SCADA: Concept of SCADA systems, Programming techniques for : Creation of pages, Sequencing of pages, Creating graphics and animation, Dynamos programming with variables, Trending, Historical data storage and Reporting, Alarm management, reporting of events and parameters. Comparison of different SCADA packages. Application Development using SCADA system.

UNIT – III **9**

DCS Introduction: Location of DCS in Plant, functions, advantages and limitations, Comparison of DCS with PLC. DCS components/ block diagram, Architecture, Functional requirements at each level. Layout of DCS, Controller Details, Redundancy, I/O Card Details, Junction Box and Marshalling Cabinets.

UNIT – IV **9**

Distributed Control System: Distributed Control Systems (DCS) – Difference between SCADA system and DCS – local control unit – programming language – communication facilities – operator interface – engineering interfaces.

UNIT – V **9**

Applications: Applications of SCADA and DCS – Case studies of Process plants using SCADA and DCS – Advanced features / options in SCADA and DCS – Role of PLC in DCS and SCADA – comparison – field devices (Transducers, drives etc) in DCS / SCADA.

Total: 45

REFERENCES:

1. Lukas Michael P., "Distributed Control Systems", Van Nostrand Reinfold Company, 2002.
2. Dobrivojie Popovic and Vijay P. Bhatkar, "Distributed Computer Control for Industrial Automation", CRC Press, 1990.
3. CIMPLICITY SCADA Packages Manual Fanuc India Ltd., 2004.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	demonstrate the basic concepts on automation system	Understanding (K2)
CO2:	develop programming with SCADA system	Applying (K3)
CO3:	compare and explain the basic concepts of DCS and SCADA	Applying (K3)
CO4:	develop a DCS and SCADA system for a process to meet a set of specifications	Applying (K3)
CO5:	apply the SCADA and DCS in various industrial applications	Analyzing (K4)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3
CO1	1	1	2
CO2	2		3
CO3	1	1	2
CO4	2		3
CO5	3		3

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

18AEE11 INDUSTRIAL ELECTRONICS

(Common to Applied Electronics & Mechatronics branches)

L	T	P	Credit
3	0	0	3

Preamble	This course brings an overview of power converters and its applications towards industrial perspective. It also includes the various control and protection techniques for converters.
Prerequisites	Electron Devices, Electrical Machines, Power Electronics

UNIT – I **9**

Power Semiconductor Devices: Principle of operation and characteristics of power diodes, SCR, TRIAC, GTO, Power BJT, Power MOSFET and IGBT – Thyristor protection circuits.

UNIT – II **9**

Phase Controlled Rectifiers: Single phase half and full converters – Three phase half and full converters – Triggering circuits. Inverters: Single phase and three phase inverters – Types of PWM techniques: Sinusoidal PWM, modified sinusoidal PWM and multiple PWM.

UNIT – III **9**

DC-DC Converters: Chopper: Principle of operation – Step up and step down chopper – Control strategies – Voltage, Current and Load commutated chopper.

UNIT – IV **9**

AC-AC Converters: Principle of single phase AC voltage controller – Phase control – ON-OFF control. Cycloconverters: Step up and step down operation - Three phase to single phase and three phase to three phase cycloconverters - Introduction to Matrix Converters

UNIT-V **9**

Solid State DC and AC Drives: DC Drives: Conventional speed control methods for DC motors – DC motor control using rectifiers and choppers – AC drives: Conventional speed control methods for AC motors – Control of induction motor by Voltage, frequency, V/f and slip power recovery scheme. Speed control methods of single phase induction motors and synchronous motors.

Total: 45

REFERENCES:

1. Muhammad H. Rashid, "Power Electronics: Circuits Devices and Applications", 3rd Edition, Pearson Education, 2003.
2. Khanchandani K.B. and Singh M.D., "Power Electronics", 2nd Edition, Tata McGraw Hill Publishers, New Delhi, 2006.
3. Gopal K. Dubey, "Fundamentals of Electrical Drives", 2nd Edition, Narosa Book Distributors Pvt. Ltd, 2012.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	understand the operation and characteristics of basic power semiconductor devices	Understanding (K2)
CO2:	demonstrate the various PWM techniques for inverter and converter operations	Applying (K3)
CO3:	explicate the principle and operation of choppers	Understanding (K2)
CO4:	summarize the types and operation of AC-AC converters	Understanding (K2)
CO5:	experiment with various speed control methods with respect to industrial applications	Applying (K3)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3
CO1	3		2
CO2	2		2
CO3	3		3
CO4	2	1	2
CO5	3		2

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy