KONGU ENGINEERING COLLEGE
PERUNDURAI ERODE – 638 060
(Autonomous)

VISION

To be a centre of excellence for development and dissemination of knowledge in Applied Sciences, Technology, Engineering and Management for the Nation and beyond.

MISSION

We are committed to value based Education, Research and Consultancy in Engineering and Management and to bring out technically competent, ethically strong and quality professionals to keep our Nation ahead in the competitive knowledge intensive world.

QUALITY POLICY

We are committed to

- Provide value based quality education for the development of students as competent and responsible citizens.
- Contribute to the nation and beyond through research and development
- Continuously improve our services

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VISION

To be a centre of excellence for development and dissemination of knowledge in Electronics and Communication Engineering for the Nation and beyond

MISSION

Department of Electronics and Communication Engineering is committed to:

MS1: To impart industry and research based quality education for developing value based electronics and communication engineers
MS2: To enrich the academic activities by continual improvement in the teaching learning process
MS3: To infuse confidence in the minds of students to develop as entrepreneurs
MS4: To develop expertise for consultancy activities by providing thrust for Industry Institute Interaction
MS5: To endeavour for constant upgradation of technical expertise for producing competent professionals to cater to the needs of the society and to meet the global challenges

2018 REGULATIONS

PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

Graduates of **M.E –Embedded Systems** will

PEO1: Succeed in industry and research by applying knowledge of digital systems, embedded systems, signal and image processing and networking.
PEO2: Identify, design and analyze solutions to solve real world problems in embedded domain
PEO3: Demonstrate soft skills , professional and ethical values and aptitude for life long learning needed for a successful professional career

MAPPING OF MISSION STATEMENTS (MS) WITH PEOs

MS\PEO	PEO1	PEO2	PEO3
MS1	3	3	3
MS2	2	2	3
MS3	3	3	3
MS4	3	3	1
MS5	2	2	3

1 – Slight, 2 – Moderate, 3 – Substantial

PROGRAM OUTCOMES (POs)

M.E (Embedded Systems) Graduates will be able to:

PO1 Independently carry out research/investigation and development work to solve practical problems

PO2 Write and present a substantial technical report/document

PO3 Apply the knowledge of digital system, embedded systems, signal & image processing and networking to provide solutions for real time embedded applications

PO4 Use research based knowledge includes design, analyze and interpret data for Automotative Electronics, Consumer Electronics, Robotics, Automation and Process Control Industries to undertake multi disciplinary industrial projects and solve complex problems using modern tools.

PO5 Demonstrate self confidence and communication skills to become an efficient team leader

PO6 Continue to improve the professional value through lifelong learning and hold ethical responsibility for the professional and the society at large

MAPPING OF PEOs WITH POs AND PSOs

PEO\PO	PO1	PO2	PO3	PO4	PO5	PO6
PEO1	3	3	3	3	2	2
PEO2	3	2	3	3	2	2
PEO3	3	1	2	2	3	3

1 – Slight, 2 – Moderate, 3 – Substantial

CURRICULUM BREAKDOWN STRUCTURE UNDER REGULATION 2018

Curriculum Breakdown Structure(CBS)	Curriculum Content (% of total number of credits of the program)	Total number of contact hours	Total number of credits
Program Core(PC)	41.67	450	30
Program Electives(PE)	25	270	18
Humanities and Social Sciences and Management Studies(HSMS)	5.56	60	4
Project(s)/Internships(PR)/Others	27.7	300	20
Total			**72**

KEC R2018: SCHEDULING OF COURSES – ME (Embedded Systems)

Semester	Theory/ Theory cum Practical / Practical							Internship & Projects	Special Courses	Credits
	1	2	3	4	5	6	7	8	9	
I	Applied Mathematics for Electronic Engineers HSMS-1 (3-1-0-4)	Design of Embedded Systems PC-1 (3-0-0-3)	Digital System Design for Embedded Systems PC-2 (3-1-0-4)	Sensors and Actuators For Robotics PC-4 (3-0-0-3)	Programming Languages for Embedded Systems PC-3 (3-0-2-4)	Microcontroller System Design PC-5 (3-0-2-4)				22
II	Embedded Networking and Buses PC-6 (3-0-2-4)	RISC Processor PC-7 (3-0-2-4)	Embedded Linux PC-8 (3-0-2-4)	Professional Elective I PE-1 (3-0-0-3)	Professional Elective II PE-2 (3-0-0-3)	Professional Elective III PE-3 (3-0-0-3)		Mini Project PR-1 (0-0-4-2)		23
III	Professional Elective I PE-4 (3-0-0-3)	Professional Elective II PE-5 (3-0-0-3)	Professional Elective III PE-6 (3-0-0-3)					Project work Phase – I PR-2 (0-0-12-6)		15
IV								Project work Phase – II PR-2 (0-0-24-12)		12

Total Credits: 72

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M.E. DEGREE IN EMBEDDED SYSTEMS

CURRICULUM

(For the candidates admitted from academic year 2018-19 onwards)

SEMESTER – I

Course Code	Course Title	Hours / Week			Credit	Maximum Marks			CBS
		L	T	P		CA	ESE	Total	
	Theory/Theory with Practical								
18AMT13	Applied Mathematics for Electronics Engineers	3	1	0	4	50	50	100	PC
18EST11	Design of Embedded Systems	3	0	0	3	50	50	100	PC
18EST12	Digital System Design for Embedded Systems	3	1	0	4	50	50	100	PC
18EST13	Sensors and Actuators for Robotics	3	0	0	3	50	50	100	PC
18ESC11	Programming Languages for Embedded Systems	3	0	2	4	50	50	100	PC
18ESC12	Microcontroller System Design	3	0	2	4	50	50	100	PC
	Total				**22**				

CA – Continuous Assessment, ESE – End Semester Examination, CBS – Curriculum Breakdown Structure

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M.E. DEGREE IN EMBEDDED SYSTEMS

CURRICULUM

(For the candidates admitted from academic year 2018-19 onwards)

SEMESTER – II

CBS	Course Title	Hours / Week			Credit	Maximum Marks		
		L	T	P		CA	ESE	Total
	Theory/Theory with Practical							
18ESC21	Embedded Networking and Buses	3	0	2	4	50	50	100
18ESC22	RISC Processor	3	0	2	4	50	50	100
18ESC23	Embedded Linux	3	0	2	4	50	50	100
	Elective I	3	0	0	3	50	50	100
	Elective II	3	0	0	3	50	50	100
	Elective III	3	0	0	3	50	50	100
	Practical							
18ESP21	Mini project	0	0	4	2	100	0	100
	Total				**23**			

CA – Continuous Assessment, ESE – End Semester Examination, CBS-Curriculum Breakdown Structure

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M.E. DEGREE IN EMBEDDED SYSTEMS

CURRICULUM

(For the candidates admitted from academic year 2018-19 onwards)

SEMESTER – III

Course Code	Course Title	Hours / Week			Credit	Maximum Marks			CBS
		L	T	P		CA	ESE	Total	
	Theory/Theory with Practical								
	Elective - IV	3	0	0	3	50	50	100	PE
	Elective - V	3	0	0	3	50	50	100	PE
	Elective - VI	3	0	0	3	50	50	100	PE
	Practical								
18ESP31	Project Work Phase I	0	0	12	6	50	50	100	PR
	Total				**15**				

CA – Continuous Assessment, ESE – End Semester Examination, CBS – Curriculum Breakdown Structure

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M.E. DEGREE IN EMBEDDED SYSTEMS

CURRICULUM

(For the candidates admitted from academic year 2018-19 onwards)

SEMESTER – IV

Course Code	Course Title	Hours / Week			Credit	Maximum Marks			CBS
		L	T	P		CA	ESE	Total	
	Practical								
18ESP41	Project Work Phase II	0	0	24	12	50	50	100	PR
	Total				**12**				

CA – Continuous Assessment, ESE – End Semester Examination, CBS – Curriculum Breakdown Structure

Total Credits: 72

LIST OF PROFESSIONAL ELECTIVES						
Course Code	**Course Title**	**Hours/Week**			**Credit**	**CBS**
		L	**T**	**P**		
SEMESTER II						
18VLE02	Design of Semiconductor Memories	3	0	0	3	PE
18VLE06	Supervised Machine Learning Algorithms	3	0	0	3	PE
18COE09	DSP Processor Architecture and Programming	2	0	2	3	PE
18MWC22	Network Security Essentials	3	0	2	4	PE
18ESE01	Solar and Energy Storage System	3	0	0	3	PE
18ESE02	Signal and Image Processing for Embedded Applications	2	0	2	3	PE
18ESE03	QT Cross Compiling Application Development	3	0	0	3	PE
18ESE04	Verilog HDL for Embedded FPGA Processor	3	0	0	3	PE
18ESE05	Medical Imaging Systems	3	0	0	3	PE
18ESE06	Computer Based Industrial Control	3	0	0	3	PE
SEMESTER III						
18VLE12	Nature Inspired Optimization Techniques	3	0	0	3	PE
18CIE15	Virtual Instrumentation for Industrial Applications	3	0	0	3	PE
18MSE18	Design and Analysis of Algorithms	3	0	0	3	PE
18ESE07	Data Analysis for Engineering	3	0	0	3	PE
18ESE08	RTOS for Embedded Systems	2	0	2	3	PE
18ESE09	System on Chip	3	0	0	3	PE
18ESE10	Design of Embedded Control System	3	0	0	3	PE
18ESE11	Multicore Processor and Computing	3	0	0	3	PE
18ESE12	Programming Internet of Things	3	0	0	3	PE
18ESE13	Single Board Computer	2	0	2	3	PE

18AMT13 APPLIED MATHEMATICS FOR ELECTRONICS ENGINEERS

(Common to VLSI Design, Communication Systems and Embedded Systems Branches)

L	T	P	Credit
3	1	0	4

Preamble	This course will demonstrate various analytical skills in applied mathematics and use extensive mathematical tools such as linear programming, graph and queuing theory with the tactics of problem solving and logical thinking applicable in electronics engineering.
Prerequisites	Vectors and Probability

UNIT – I **9**

Vector Spaces: Definition – Subspaces – Linear dependence and independence – Basis and dimension – Row space, Column space and Null Space – Rank and nullity.

UNIT – II **9**

Linear Programming: Mathematical Formulation of LPP – Basic definitions – Solutions of LPP: Graphical method – Simplex method – Transportation Model – Mathematical Formulation - Initial Basic Feasible Solution: North west corner rule – Vogel's approximation method – Optimum solution by MODI method – Assignment Model – Mathematical Formulation – Hungarian algorithm.

UNIT – III **9**

Non-Linear Programming: Formulation of non–linear programming problem – Constrained optimization with equality constraints – Constrained optimization with inequality constraints – Graphical method of non–linear programming problem involving only two variables.

UNIT – IV **9**

Graph Theory: Introduction of graphs – Isomorphism – Subgraphs – Walks, paths and circuits – Connected graphs – Eulerian Graphs – Hamiltonian Paths and circuits – Digraph – Adjacency matrix and incidence matrix of graphs – Applications: Shortest path algorithms – Dijkstra's algorithm – Warshall's algorithm – Trees – Properties of trees – Spanning trees – Applications of trees: Minimal spanning trees – Prim's Algorithm – Kruskal's algorithm.

UNIT – V **9**

Queuing Theory: Markovian queues – Single and Multi-server Models – Little's formula – Non- Markovian Queues – Pollaczek Khintchine Formula.

Lecture:45, Tutorial:15, Total: 60

REFERENCES:

1. Howard Anton, "Elementary Linear Algebra", 10th Edition, John Wiley & Sons, 2010.
2. Kanti Swarup, Gupta P.K. and Man Mohan, "Operations Research", S. Chand & Co., 1997.
3. Bondy J.A. and Murthy, USR, "Graph Theory and Applications", Mc Millan Press Ltd., 1982.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	demonstrate accurate and efficient use of advanced algebraic techniques	Understanding (K2)
CO2:	formulate and solve linear programming problems that appear in electronics engineering	Evaluating (K5)
CO3:	use non-linear programming concepts in real life situations	Applying (K3)
CO4:	apply graph theoretic algorithms in design of systems	Applying (K3)
CO5:	analyze the characteristics of various queuing models	Analyzing (K4)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	2	3			
CO2	3		2	1		
CO3	2		3			
CO4	1		3	2		
CO5			2	3		

1 – Slight, 2 – Moderate, 3 – Substantial, BT – Bloom's Taxonomy

18EST11 DESIGN OF EMBEDDED SYSTEMS

L	T	P	Credit
3	0	0	3

Preamble	To understand the design and use of single-purpose processors, general-purpose processors and to describe memories and buses.
Prerequisites	Digital Electronics

UNIT – I **9**

Embedded Design Life Cycle: Embedded Design life cycle - Product specification - Hardware / Software partitioning - Detailed hardware and software design - Integration - Product testing Selection Processes - Microprocessor Vs Micro Controller - Performance tools - Bench marking - RTOS availability - Tool chain availability - Other issues in selection processes.

UNIT – II **9**

Partitioning Decision: Hardware / Software duality - Coding Hardware - ASIC revolution - Managing the Risk - Co-verification - Execution environment - Memory organization - System startup - Hardware manipulation - Memory mapped access - Speed and code density.

UNIT – III **9**

Emulator: Interrupt Service routines - Watch dog timers - Flash memory Basic toolset - Host Based debugging - Remote debugging - ROM emulators - logic Analyzer - Caches - Computer optimization - Statistical profiling.

UNIT – IV **9**

In Circuit Emulators: Bullet proof run control - Real time trace - Hardware break points - Overlay memory - Timing constraints - Usage issues - Triggers.

UNIT – V **9**

Testing: Bug tracking - Reduction of risks and costs - Performance - Unit testing - Regression testing - Choosing test cases - Functional tests - Coverage tests - Testing embedded software - Performance testing – Maintenance.

Total: 45

REFERENCES:

1. Arnold S. Berger, “Embedded System Design”, CMP Books, USA, 2002.
2. Sriram Iyer, “Embedded Real time System Programming”, Tata McGraw-Hill, 2008.
3. Ronald C. Arkin, “Behaviour-based Robotics”, The MIT Press, 1998.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	realize the design flow of an embedded system	Understanding (K2)
CO2:	comprehend partitioning decision involved in embedded system design	Understanding (K2)
CO3:	apply basic tool set used for debugging software and hardware	Applying (K3)
CO4:	apply the concepts of emulators in real time applications	Applying (K3)
CO5:	comprehend different testing methods involved in test phase for the design of embedded system	Applying (K3)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2		3	2	2	
CO2			2	3	1	
CO3	1		2	3		
CO4	2		2	3		
CO5			3	2		

1 – Slight, 2 – Moderate, 3 – Substantial, BT – Bloom's Taxonomy

18EST12 DIGITAL SYSTEM DESIGN FOR EMBEDDED SYSTEMS

L	T	P	Credit
3	1	0	4

Preamble	To understand the advanced digital system design principles for an embedded systems through simulation on verilog language and implementation on PLDs devices
Prerequisites	Digital Electronics, VLSI design

UNIT – I **9**

Verilog Programming: Introduction of Verilog HDL - Language Motivation - Overview of Verilog HDL - Data Types in Verilog - Abstraction Levels In Verilog - Behavioral, Gate level Data flow and Structural - Expressions - Operators, Operands and Special Consideration in Expression - System Task and Functions - Design and simulation of Adder, Multiplexer, Comparator Flipflops, Shift Registers.

UNIT – II **9**

Clocked Synchronous Sequential Circuit(CSSN): Analysis of Sequential Networks: Mealy and Moore Model, Modeling of CSSN : State Diagram, State Reduction Methods - State Assignment - Design of CSSN.

UNIT – III **9**

Asynchronous Sequential Circuit Design: Analysis of Asynchronous Sequential Circuit (ASC) - Modeling of ASC: Primitive Flow Table - Flow Table Reduction Methods - State Assignment: Races in ASC- Hazards in ASC.

UNIT – IV **9**

Fault Analytics: Introduction of Fault – Types - Fault Testing Methods: Fault Table Method - Path Sensitization Method - Boolean Difference Method - Kohavi Algorithm.

UNIT – V **9**

PLD: Introduction to PLD - Abstract and Evolution - Simple Programmable Logic Device(SPLD) - Complex Programmable Logic Device - Field Programmable Gate Array.

Lecture:45, Tutorial:15, Total: 60

REFERENCES:

1. Vivek Sagdeo, "The Complete Verilog Book", Kluwer Academic Publishers, New Delhi, 2002.
2. Givone Donald G., "Digital Principles and Design", Tata McGraw- Hill, New Delhi, 2002.
3. Biswas Nripendra N., "Logic Design Theory", Prentice Hall of India, New Delhi, 2001.
4. Vaibbhav Taraate, "PLD Based Design with VHDL - RTL Design, Synthesis and Implementation", Springer Nature, Singapore, 2017.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	interpret the syntax of verilog Programming Language with digital circuits and write verilog code for combinational and sequential circuits	Understanding (K2)
CO2:	design the synchronous sequential circuits	Creating (K6)
CO3:	design the asynchronous sequential circuits with hazards free	Creating (K6)
CO4:	identify the faults in the circuit by fault analytics algorithms	Understanding (K2)
CO5:	construct the combinational and sequential circuits using PLDs	Creating (K6)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1			3	2		
CO2			3	2		
CO3	2		2	3		
CO4	1		3	3		
CO5	2		2	3		

1 – Slight, 2 – Moderate, 3 – Substantial, BT – Bloom's Taxonomy

18EST13 SENSORS AND ACTUATORS FOR ROBOTICS

L	T	P	Credit
3	0	0	3

Preamble	To learn and analyze the parameters components of robotics such as parallel and grippers , manipulators, sensors and actuators
Prerequisites	Basic of electronics

UNIT – I **9**

Introduction to Robotics: Definition and origin of robotics - Different types of robotics - Various generations of robots - Degrees of freedom - Asimovs laws of robotics - Dynamic stabilization of robots.

UNIT – II **9**

Sensors, Actuators and Drive Systems: Sensors: Machine vision - Ranging - Laser – Acoustic – Magnetic - Fiber optic and tactile sensors. Actuators: Manipulator dynamics and force control - Electronic and pneumatic manipulator control circuits - End effectors – various types of grippers - design considerations. Drives: Hydraulic, pneumatic and electric drives

UNIT – III **9**

Robot Dynamics: Determination of HP of motor and gearing ratio - Variable speed arrangements - Path determination Solution of inverse kinematics problem - Multiple solution jacobian work envelop – Hill Climbing Techniques.

UNIT – IV **9**

Robot Programming: Introduction to robot programming languages - Classification of robot languages - Computer control and robot software - VAL system and Language.

UNIT – V **9**

Industrial Applications: Mutiple robots - Machine interface - Robots in manufacturing and non-manufacturing applications - Robot cell design - Selection of robot.

Total: 45

REFERENCES:

1. Deb S.R.,"Robotics Technology and Flexible Automation", 2nd Edition, McGrawHill Publications, 2010.
2. Mikell P., Weiss G.M., Nagel R.N. and Odraj N.G., "Industrial Robotics", McGraw-Hill, Singapore, 1996.
3. Ghosh, "Control in Robotics and Automation: Sensor Based Integration", Allied Publishers, Chennai, 1999.
4. Klafter R.D., Chimielewski T.A. and Negin M., "Robotic Engineering – An Integrated Approach", Prentice Hall of India, New Delhi, 2007.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	describe the functions of a robot	Remembering (K1)
CO2:	analyze the type of sensors, actuators and drives for robots	Analyzing (K4)
CO3:	apply the kinematics and path planning for robot applications	Applying (K3)
CO4:	experiment robot operations using VAL robot programming language	Applying (K3)
CO5:	develop robots for manufacturing Industries	Creating (K6)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1			3	2		
CO2	1		3	2		
CO3	1		3	2		
CO4			3	2		
CO5	2		2	3	1	2

1 – Slight, 2 – Moderate, 3 – Substantial, BT – Bloom's Taxonomy

18ESC11 PROGRAMMING LANGUAGES FOR EMBEDDED SYSTEMS

L	T	P	Credit
3	0	2	4

Preamble	To know about the major programming paradigms, the principles and techniques involved in embedded system design and to implement modern programming languages.
Prerequisites	Microcontroller

UNIT – I **9**

Introduction to C Language: Overview of C - Constants, Variables, and Data types - Operators and Expressions - Managing Input and Output Operations - Decision Making and Branching - Decision Making and Looping - Arrays.

UNIT – II **9**

C Programming: Character Arrays and Strings - User defined Functions - Structures and Unions – Pointers - File Management in C - Dynamic Memory Allocation and Linked Lists - The Preprocessor.

UNIT – III **9**

C++ Programming: Basics of C++ Programming-Memory Models and Namespace - Objects and Classes - Working with classes - Classes and Dynamic Memory Allocation - Class Inheritance - Reusing code in C++ - Friends – Exceptions - RTI and Type cast - String class - Input, Output and Files.

UNIT – IV **9**

Introduction to Python: Basics of Python Programming - Decision control statements - Functions and Modules - Python strings - File handling.

UNIT – V **9**

Advanced topics in Python: Data Structures - Classes and Objects - Inheritance - Operator Overloading - Error and Exception handling.

List of Exercises / Experiments :

1. C program for static and dynamic memory allocation
2. C++ program with objects to perform banking transactions
3. Python program to create text file and write content in the file
4. Python program to open a existing file and append content to the file
5. Use try and except in python while performing arithmetic division / or / while opening a file

Lecture:45, Practical:30, Total: 75

REFERENCES/ MANUALS/ SOFTWARES:

1. Balagurusamy E., "Programming in ANSI C", 7th Edition, Tata McGraw Hill Publication, 2016.
2. Reema Thareja, "Python Programming using Problem Solving Approach", 1st Edition, Oxford Publication, 2017.
3. Stanley B. Lippman, Josee Lajoie, Barbara E. Moo, "C++ Primer", 4th Edition, Pearson Education, 2007.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	manipulate data, process I/O and convert numerical values using C	Applying (K3)
CO2:	apply advanced data structures for problem solving	Applying (K3)
CO3:	solve problems using object oriented programs in C++	Applying (K3)
CO4:	apply python programming concepts for data manipulation	Applying (K3)
CO5:	use python programs with object oriented and exception handling features and differentiate interpreted language(Python) from compiled languages(C, C++)	Applying (K3)
CO6:	distinguish static and dynamic memory allocation in C programming	Analyzing (K4), Manipulation (S2)
CO7:	use C++ programming for implementing objects and Inheritance	Applying (K3), Manipulation (S2)
CO8:	apply python programming concepts for file operations and exception handling	Applying (K3), Precision (S3)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2		3	3		
CO2	2		2	3		
CO3	2		2	3		
CO4	2		3	2		
CO5	2		1	3		
CO6	2		2	3		
CO7	2		2	3		
CO8	2		2	3		

1 – Slight, 2 – Moderate, 3 – Substantial, BT – Bloom's Taxonomy

18ESC12 MICROCONTROLLER SYSTEM DESIGN

L	T	P	Credit
3	0	2	4

Preamble	To expertise assembly level and C level program for the basic 8051 and pic16F8777A microcontroller architecture and able to interface sensors and motors for project development
Prerequisites	Digital Electronics

UNIT – I **9**

8051 Architecture: Architecture - Memory organization - Addressing modes - Instruction set - Timers - Counters- Interrupts - I/O ports - Serial Communication.

UNIT – II **9**

8051 Programming: Assembly Language Programming - Timer Counter Programming - Serial Communication Programming - Interrupt Programming - Interfacing I/O Devices - RTOS for 8051- RTOSLite - FullRTOS - Task creation and Run - LCD digital clock/thermometer using FullRTOS.

UNIT – III **9**

PIC Microcontroller: Architecture of PIC18FXX - Memory organization - Addressing modes - Instruction set - I/O ports - Simple Assembly Language Programming - Introduction to Embedded C.

UNIT – IV **9**

Peripheral of PIC Microcontroller and Programming: I/O Port - Timers - I2C bus - A/D Converter - UART- CCP Modules - Interrupts - EEPROM Memories.

UNIT – V **9**

Hardware Interfacing: LCD Display - Touch Screen - Keypad - SPI Bus Protocol - DS1307 RTC - DC Motor Direction and Speed control using PWM - Stepper Motor.

List of Exercises / Experiments :

1. Introduction to Proteus – Simple programs using ALP.
2. LED/ Switch/ Keypad /Relay/LCD - interfacing using 89c51 Microcontroller.
3. Introduction to CCS Compiler – Simple programs using Embedded C.
4. Timer-External hardware Interrupt - A/D converter - Serial Communication – 3pin Temperature Sensor Interfacing.
5. Mini Project using DS1307 RTC/DC Motor/Stepper Motor

Lecture:45, Practical:30, Total: 75

REFERENCES / MANUALS / SOFTWARES:

1. Muhammad Ali Mazidi, Janice G. Mazidi and Rolin D McKinlay, "The 8051 Microcontroller and Embedded Systems", Prentice Hall, 2005.
2. Muhammad Ali Mazidi, Rolin D. McKinlay, Danny Causy, "PIC Microcontroller and Embedded Systems using Assembly and C for PIC18", Pearson Education, 2008.
3. MykePredko, "Programming and Customizing the 8051 Microcontroller", Tata McGraw Hill, 2001.
4. John Lovine, "PIC Microcontroller Project Book", McGraw Hill, 2000.
5. Proteus Simulator

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	describe the architecture of 8051 and rewrite assembly language program for arithmetic and logical operations	Understanding (K2)
CO2:	apply assembly language program for internal peripherals of 8051 microcontroller using proteus simulator	Applying (K3)
CO3:	demonstrate the concepts of RTOS for 8051 microcontroller and architecture of PIC18Fxx	Applying (K3)
CO4:	describe the architecture of PIC18Fxx and rewrite assembly language program for arithmetic and logical operations	Understanding (K2)
CO5:	develop embedded C program for interrupt, ADC and Serial communication using CCS compiler	Applying (K3)
CO6:	use 8051 ALP to interface LED, switch, keypad and LCD	Applying (K3), Manipulation (S2)
CO7:	make use of C programming language to perform timer, external hardware interrupt and serial communication	Applying (K3), Manipulation (S2)
CO8:	design a Project using DS1307 RTC/ DC Motor/ Stepper Motor/ sensor interfacing	Creating (K6), Precision (S3)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1			3	2		
CO2			3	3		
CO3	1		3	2		
CO4			3	2		
CO5	2		3	3		
CO6	2		3	2		
CO7	2		3	2		
CO8	3	3	3	3	2	2

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

18ESC21 EMBEDDED NETWORKING AND BUSES

L	T	P	Credit
3	0	2	4

Preamble	To understand the concepts and principles of various buses and networks for embedded applications with respect ISO/OSI standards.
Prerequisites	Fundamentals of Microcontrollers and Networks

UNIT – I **9**

Embedded Communication: Modern Instrumentation and Control Systems - Introduction to Networks- Advantages and Disadvantages. OSI Model - Foundations of OSI Model. Protocol - Standards. Grounding, Shielding and Noise.

UNIT – II **9**

Embedded Networking: Introduction – Serial/Parallel Communication – Serial communication protocols: - RS232 standard – RS485 – Synchronous Serial Protocols -Serial Peripheral Interface (SPI)– Inter Integrated Circuits (I2C)– PC Parallel port programming -ISA/PCI Bus protocols.

UNIT – III **9**

USB Protocol: Firewire USB bus – Introduction – Speed Identification on the bus – USB States – USB bus communication: Packets – Data flow types – Enumeration – Descriptors.

UNIT – IV **9**

Industrial Ethernet: Introduction-IEEE Standards-Ethernet MAC layer-IEEE 802.2 and Ethernet SNAP- OSI and IEEE 802.3 standard. Ethernet transceivers, Ethernet types, switches & switching hubs, 10 Mbps Ethernet, 100 Mbps Ethernet, Gigabit Ethernet. TCP / IP Overview- Internet Layer Protocols-Host-to-Host layer.

UNIT – V **9**

Devicenet: Overview – Layers Profibus-Overview-Protocol Stack. HART Protocol – Overview- Layers. Foundation Field Bus- Layers-Error Detection and Diagnostics. CAN Bus – Introduction - Frames –Bit stuffing –Types of errors –Nominal Bit Timing –PIC18Fxx microcontroller CAN Interface.

List of Exercises / Experiments:

1. Basics of Digital Modulation techniques(Simulation)
2. Serial port programming RS232- SPI (Hardware)
3. PIC18Fxx Microcontroller USB Interface (Simulation/Hardware)
4. TCP / IP (Simulation/Hardware)
5. A simple CAN interface based application using PIC18Fxx microcontroller (Simulation/Hardware)

Lecture:45, Practical:30, Total: 75

REFERENCES / MANUALS / SOFTWARES:

1. Steve Mackay, Edwin Wright, John Park and Deon Reynders, "Practical Industrial Data Networks: Design, Installation and Trouble Shooting", 1st Edition, Newnes Books, 2004.
2. William Buchanan, "Computer Buses-Design and Application", CRC Press, 2000.
3. Frank Vahid, Tony, Givargis, "Embedded Systems Design: A Unified Hardware/Software Introduction", 3rd Edition, Wiley Publications, 2009.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	realize the embedded communication based on OSI model standard and digital modulation techniques to examine the requirements of today's digital world	Applying (K3)
CO2:	differentiate serial communication and parallel communication	Understanding (K2)
CO3:	develop a system to transfer data between peripheral device and microcontroller through USB protocol	Applying (K3)
CO4:	analyze the different IEEE Standards, challenges and its solutions in wireless networks	Analyzing (K4)
CO5:	demonstrate a comprehensive theoretical and practical knowledge of the key elements and principles of operation of commonly used automotive networks including: Profibus, HART and CAN bus	Applying (K3)
CO6:	demonstrate signal generation and detection using digital modulation techniques	Applying (K3), Manipulation (S2)
CO7:	carryout interfacing of serial port, USB and CAN with microcontroller	Applying (K3), Manipulation (S2)
CO8:	analyze the efficiency of a embedded systems over TCP/IP communication	Analyzing (K4), Precision (S3)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1			3	2		
CO2			3	2		
CO3			3	3		
CO4	1		3	3		
CO5	1		3	3		
CO6	2		3	3		
CO7	2		3	3		
CO8	2		3	3		

1 – Slight, 2 – Moderate, 3 – Substantial BT – Bloom's Taxonomy

18ESC22 RISC PROCESSOR

L	T	P	Credit
3	0	2	4

Preamble	To design the embedded system applications with AVR and ARM microprocessors employing the knowledge of different user peripherals and operating systems.
Prerequisites	Microprocessor

UNIT – I **9**

AVR Microcontroller Architecture: Architecture – memory organization – addressing modes – I/O Memory – EEPROM – I/O Ports-SRAM –Timer –UART – Interrupt Structure- Serial Communication with PC – ADC/DAC Interfacing.

UNIT – II **9**

ARM Architecture and Programming: Acorn RISC Machine -Core & Architectures -- The ARM Programmer's model -Registers – Pipeline - Interrupts - Coprocessors. Instruction set – Thumb instruction set – Instruction cycle timings System Peripherals: Bus structure –Memory map –Memory accelerator module – External bus interface –Phase Locked Loop –VLSI peripheral bus divider –Power control

UNIT – III **9**

User Peripherals: Pin connect block –General purpose I/O –Timers –Capture –Compare –PWM modules– Watchdog timer –Analog to digital converter-UART –I2C interface –SPI interface –CAN interface

UNIT – IV **9**

Memory Protection and Management: Protected Regions-Initializing MPU, Cache and Write Buffer-MPU to MMU-Virtual Memory-Page Tables- TLB-Domain and Memory Access Permission-Fast Context Switch Extension.

UNIT – V **9**

ARM Application Development: Introduction to DSP on ARM – Filter –Exception Handling – Interrupts – Interrupt handling schemes- Firmware and boot loader – Example: Standalone - Embedded Operating Systems – Fundamental Components.

List of Exercises / Experiments :

1. Interfacing analog sensor/ GSM with ATmega2560 or Arduino
2. Understanding Keil IDE and Keil based PLL and VPB configurations
3. Interfacing Servo motor/ RTC with LPC21xx.
4. SLOS-I on ARM LPC21xx
5. SLOS-II on ARM LPC21xx

Lecture:45, Practical:30, Total: 75

REFERENCES / MANUALS / SOFTWARES:

1. Andrew N. Sloss, Dominic Symes, Chris Wright, John Rayfield, "ARM System Developer's Guide Designing and Optimizing System Software", Elsevier, 2007.
2. Dananjay V. Gadre, "Programming and Customizing the AVR Microcontroller", McGraw Hill, 2017.
3. Trevor Martin, "The Insider's Guide To The Philips ARM7-Based Microcontrollers, An Engineer's Introduction To The LPC2100 Series", Hitex (UK) Ltd, 1st Reprint, April 2005.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level) S1**
CO1:	use timer, UART and ADC modules of Atmega2560 microcontroller for I/O applications	Applying (K3)
CO2:	realize the architecture and instruction set of ARM7	Applying (K3)
CO3:	use configurations of PLL and bus structures in LPC21xx for frequency generations	Applying (K3)
CO4:	differentiate MMU, MPU and Virtual Memory concepts	Understanding (K2)
CO5:	interpret the concepts of Embedded Operating Systems	Applying (K3)
CO6:	design and interface peripheral devices with LPC21xx for industrial applications	Applying (K3), Manipulation (S2)
CO7:	carryout interfacing of analog sensors with ATmega2560	Applying (K3), Manipulation (S2)
CO8:	develop OS based applications for ARM7	Applying (K3), Precision (S3)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1		3	2		
CO2			3	2		
CO3			2	3		
CO4			3	2		
CO5	1		3	2		
CO6	2		3	3	1	
CO7	2		3	3	1	
CO8	2		3	3	1	2

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

18ESC23 EMBEDDED LINUX

L	T	P	Credit
3	0	2	4

Preamble	To study and apply concepts relating to operating systems, such as concurrency and control of asynchronous processes, deadlocks, memory management, processor and disk scheduling, parallel processing, and file system organization
Prerequisites	Basics of C

UNIT – I **9**

Fundamentals of Linux: Basic Linux System Concepts: Working with Files and Directories - Introduction to Linux File system - Basic Linux commands and concepts Logging in - Shells - Basic text editing - Advanced shells and shell scripting Linux File System Linux programming - Processes and threads in Linux - Inter process communication -Linux System calls.

UNIT – II **9**

Various Distributions And Cross Platform Tool Chain: Introduction - History of Embedded Linux - Embedded Linux versus Desktop Linux -Commercial Embedded Linux Distribution - Choosing a distribution - Embedded Linux Distributions - Architecture of Embedded Linux - Linux kernel architecture - User space Linux startup sequence - GNU cross platform Tool chain.

UNIT – III **9**

Host-Target Setup and Overall Architecture: Real Life Embedded Linux Systems - Design and Implementation Methodology - Types of Host/Target Development Setups - Types of Host/Target Debug Setups - Generic Architecture of an Embedded Linux System - System Startup - Types of Boot Configurations System Memory.

UNIT – IV **9**

Kernel Configuration and Root File System: Selecting a Kernel - Configuring the Kernel - Compiling the Kernel - Installing the Kernel - Basic Root File system Structure - Libraries - Kernel Modules and Kernel Images - Device Files - Main System Applications - System Initialization - Setting Up the Bootloader U-boot.

UNIT – V **9**

Embedded Storage and Driver: Memory Technology Device (MTD) MTD Architecture - MTD Driver for NOR Flash The Flash Mapping drivers MTD Block and character devices mtdutils package Embedded File Systems Optimizing storage space-Porting Roadmap Linux serial driver Ethernet driver USB gadgets Watchdog timer Kernel Modules.

List of Exercises / Experiments :

1. Linux file access and shell scripting
2. Installation of Embedded linux distribution and tool chain for the specified target board
3. Target Development setup and Boot Configurations
4. Compiling a kernel, Building a kernel, Configuring kernel modules ,Images for specified target Board
5. Loading the images in Flash memory through JTAG and driver modules

Lecture:45, Practical:30, Total: 75

REFERENCES / MANUALS / SOFTWARES:

1. Paul Cobbaut, “Mastering Linux Fundamentals”, Art Power International Publications, 2016.
2. Karim Yaghmour, “Building Embedded Linux Systems”, 2nd Edition, O'Reilly Publications, 2008.
3. Raghavan P., Amol Lad, Sriram Neelakandan, “Embedded Linux System Design and Development”, Auerbach Publications, 2006.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	list the fundamentals of an linux OS	Remembering (K1)
CO2:	inspect kernel modules for customer peripherals	Analyze (K4)
CO3:	demonstrate communication between kernel space and user space	Applying (K3)
CO4:	develop system configuration and boot process	Applying (K3)
CO5:	inspect software tools for the development of an embedded linux system and architecture	Analyzing (K4)
CO6:	compute Linux file access and scripting	Applying (K3), Manipulation (S2)
CO7:	carryout Boot configurations and develop tool chain for specified target board	Applying (K3), Manipulation (S2)
CO8:	integrate images and target board using debugger and drivers through kernel	Analyzing (K4), Precision (S3)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1			3	2		
CO2	2		3	3		
CO3			3	2		
CO4			3	3		
CO5			3	2		
CO6	1		3	3		
CO7	2		3	3		
CO8	2		3	2	1	2

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

18VLE02 DESIGN OF SEMICONDUCTOR MEMORIES

(Common to VLSI Design and Embedded Systems branches)

L	T	P	Credit
3	0	0	3

Preamble	To study the architectures for SRAM and DRAM, various non-volatile memories, fault modeling and testing of memories for fault detection and the radiation hardening process and issues for memory.
Prerequisites	Solid State Devices

UNIT – I **9**

Random Access Memory Technologies: SRAM Cell Structures-MOS SRAM Architecture-MOS SRAM Cell and Peripheral Circuit Operation- Bipolar SRAM Technologies-Silicon On Insulator (SOl) Technology-Advanced SRAM Architectures and Technologies-Application Specific SRAMs DRAM Technology Development- CMOS DRAMs- DRAMs Cell Theory and Advanced Cell Structures- BiCMOS, DRAMs-Soft Error Failures in DRAMs- Advanced DRAM Designs and Architecture- Application Specific DRAMs.

UNIT – II **9**

Nonvolatile Memories : Masked Read-Only Memories (ROMs)- High Density ROMs- Programmable Read-Only Memories (PROMs)- Bipolar PROMs- CMOS PROMs- Erasable(UV) Programmable Road-Only Memories (EPROMs)- Floating-Gate PROM Cell- One-Time Programmable (OTP) EPROMS- Electrically Erasable PROMs (EEPROMs)- EEPROM Technology and Architecture- Nonvolatile SRAM- Flash Memories (EPROMs or EEPROM)- Advanced Flash Memory Architecture.

UNIT – III **9**

Memory Fault Modeling And Testing: RAM Fault Modeling, Electrical Testing, Peusdo Random Testing-Megabit DRAM Testing- Nonvolatile Memory Modeling and Testing- IDDQ Fault Modeling and Testing-Application Specific Memory Testing.

UNIT – IV **9**

Semiconductor Memory Reliability: General Reliability Issues- RAM Failure Modes and Mechanism-Nonvolatile Memory Reliability- Reliability Modeling and Failure Rate Prediction- Design for Reliability-Reliability Test Structures- Reliability Screening and Qualification.

UNIT – V **9**

Packaging Technologies: Radiation Effects- Single Event Phenomenon (SEP)- Radiation Hardening Techniques- Radiation Hardening Process and Design Issues- Radiation Hardened Memory Characteristics-Radiation Hardness Assurance and Testing - Radiation Dosimetry-Water Level Radiation Testing and Test Structures. Ferroelectric Random Access Memories (FRAMs)- Gallium Arsenide (GaAs) FRAMs- Analog Memories- Magnetoresistive Random Access Memories (MRAMs)- Experimental Memory Devices. Memory Hybrids and MCMs (2D)-Memory Stacks and MCMs (3D)-Memory MCM Testing and Reliability Issues-Memory Cards- High Density Memory Packaging Future Directions.

Total: 45

REFERENCES:

1. Sharma K. Ashok, “Semiconductor Memories: Technology, Testing, and Reliability”, Wiley-IEEE Press, New York, 2002.
2. Sharma K. Ashok, “Advanced Semiconductor Memories, Architectures, Designs and Applications”, Wiley-IEEE Press, New York, 2009.
3. Krzysztof Hiewski, Santosh K. Kurinec, “Nanoscale Semiconductor Memories”, CRC Press, 2017.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	comprehend the micro level operations of random access memories	Understanding (K2)
CO2:	analyze the need of non-volatile memories and their applications	Analyzing (K4)
CO3:	design the fault free memory systems by fault modeling techniques	Evaluating (K5)
CO4:	analyze and design the memory architectures by considering the radiation effects	Analyzing (K4)
CO5:	identify the packages for memories	Understanding (K2)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	2	2	2	3
CO2			2	3	2	
CO3			1	2	1	
CO4			2	3	2	
CO5	3	3	2	2	2	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

18VLE06 SUPERVISED MACHINE LEARNING ALGORITHMS

(Common to VLSI Design & Embedded Systems branches)

L	T	P	Credit
3	0	0	3

Preamble	To focus on supervised machine learning algorithms to create simple, interpretable models to solve classification and regression problem.
Prerequisites	Linear Algebra, calculus

UNIT – I **9**

Discriminative Algorithms: Cost function –LMS Algorithm – The normal Equations-Probability interpretation-locally weighted linear regression-logistic regression-generalized linear models-Application to prediction.

UNIT – II **9**

Generative Algorithms: Generative Models: Gaussian Discriminant Analysis(GDA)-Naïve Bayes- Laplace smoothing-Marginal classifier: Support Vector Machine (SVM) as optimal Margin classifier-Application to Classification.

UNIT – III **9**

Neural Networks: ANN Architecture- Parameter Initialization -Forward Propagation- Activation Functions (Sigmoid,tanh,relu)-Training and Optimization with back propagation-Learning Boolean Functions.

UNIT – IV **9**

Convolutional Neural Networks (CNN) : Convolution kernel-Pooling (Max Pooling, fractional Pooling)-Strides-Fully Connected Layers –Loss functions – MiniBatch Training -Optimization – Application to MNIST image classification.

UNIT – V **9**

Hyper Parameter Tuning: Regularization: Bias-Variance-Bias-variance Trade off- Initialization of parameters (Xavier)-Cross Validation-Data Augmentation-dropouts-Batch Normalization.

Total: 45

REFERENCES:

1. Christopher M. Bishop, "Pattern Recognition and Machine Learning", Springer-Verlag New York, Reprint, 2010.
2. Trevor Hastie, "The Elements of Statistical Learning: Data Mining, Inference, and Prediction", 2nd Edition, Springer, 2009.
3. UCI Machine Learning repository: http://archive.ics.uci.edu/ml/index.php

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	analyse and apply discriminative algorithms for classification and regression problems	Analyzing (K4)
CO2:	validate a generative model based algorithm for classification and regression problems	Analyzing (K4)
CO3:	analyse the designed ANN for a real time application using BPN	Analyzing (K4)
CO4:	develop a CNN model for image analysis	Applying (K3)
CO5:	analyse various error metrics used in supervised learning	Analyzing (K4)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1			2	3	2	
CO2			2	3	2	
CO3			2	3	2	
CO4			3	3	3	
CO5			2	3	2	

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

18COE09 DSP PROCESSOR ARCHITECTURE AND PROGRAMMING

(Common to Communication Systems,VLSI Design & Embedded Systems branches)

L	T	P	Credit
2	0	2	3

Preamble	To design the parameters of filters and implement it in real time DSP hardware.
Prerequisites	Digital Signal Processing

UNIT – I **6**

Fundamentals of Programmable DSPs: Multiplier and Multiplier accumulator (MAC) – Modified Bus Structures and Memory access in Programmable DSPs – Multiple access memory – Multi-port memory – VLIW architecture- Pipelining – Special Addressing modes in P-DSPs – On chip Peripherals

UNIT – II **6**

TMS320C54XX: Fundamentals of Programmable DSPs - Architecture of TMS320C54X-54X Buses-Memory organization-Computational Units-Pipeline operation-On-chip peripherals – Address Generation Units- Addressing modes and instruction set- assembly language instructions -Introduction to Code Composer studio

UNIT – III **6**

TMS320C6X: Architecture of TMS320C6X – Computational units-Addressing modes –Memory architecture- pipeline operation- instruction set- assembly language instructions

UNIT – IV **6**

Blackfin Processor(BF537): Architecture of BF537- Computational units - Internal Memory organization-System interrupts – Direct Memory Access- on-chip peripherals-ALU-MAC-DAG Units-Addressing modes-Assembly language instructions- Timers –Interrupts-Serial ports-UART-Simple programs

UNIT – V **6**

Applications Using TMS320C54X/C6X/BF537: Program development - Software Development Tools- The Assembler and the Assembly Source File Filter design- Linker and Memory Allocation -DSP Software Development Steps- Speech Digitization-Encoding and Decoding-Image compression-Restoration-Adaptive Echo cancellation-Modulation

List of Experiments:

1. Basic Signal operations using 54x.
2. Convolution using c54x and c6713x
3. FIR and IIR filter using C6713
4. Basic operations and convolution using BF 537
5. Speech and Audio application development using BF537

Lecture:30, Practical:30, Total: 60

REFERENCES / MANUALS / SOFTWARES:

1. Sen M. Kuo, Woon–Seng S. Gan, “Digital Signal Processors: Architecture, Implementation and Applications”, 1st Edition, Prentice Hall, 2009.
2. Woon-Seng Gan, Sen M. Kuo, “Embedded Signal Processing with the Microsignal Architecture”, John Wiley & Sons Inc. Publications, 2007.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	infer the basic concepts of DSP processor	Understanding (K2)
CO2:	apply programming concepts to develop simple and real time applications programs using c54x processor	Applying (K3)
CO3:	apply programming concepts to develop simple and real time applications using c6x processor	Applying (K3)
CO4:	apply programming concepts to develop simple and real time applications using BF 537 processor	Applying (K3)
CO5:	analyze the performance of DSP processors like TMS320C54X/C6X/BF537	Analyzing (K4)
CO6:	demonstrate the concepts of DSP using DSP processor	Applying (K3), Manipulation (S2)
CO7:	design digital filters using DSP processors	Applying (K3), Manipulation (S2)
CO8:	demonstrate speech/audio applications using DSP processor	Applying (K3), Manipulation (S2)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3				2	
CO2	3				3	
CO3	3				3	
CO4	3				3	
CO5	3	3			3	
CO6	3				3	
CO7	3				3	
CO8	3				3	

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

18MWC22 NETWORK SECURITY ESSENTIALS

(Common to Information Technology (Information Cyber Warfare), Communication Systems & Embedded Systems branches)

L	T	P	Credit
3	0	2	4

Preamble	To introduce the security problems associated with malicious software and intruders and familiarize the network security controls that help to protect the usability, integrity, reliability and safety of the network infrastructure and the data that travels through it.
Prerequisites	Computer Networks

UNIT – I **9**

Introduction: Characteristics of Networks, Need for network security, Intruders, Malicious Software, Reconnaissance, Eavesdropping, wiretapping, impersonation, traffic analysis, website defacement, DOS, active code or mobile code attacks, OSI Security Architecture, Security Services, Model for Network Security.

UNIT – II **9**

Cryptography and Key Distribution: Classical Encryption Techniques, Symmetric Encryption Principles, Symmetric Encryption Algorithms, DES, AES, Stream Ciphers, Block Cipher Modes of Operation, Public Key Cryptography Principles, Public Key Cryptographic Algorithms, RSA,ECC, Key Distribution using Symmetric and Asymmetric Encryption, Kerberos, X.509, Public Key Infrastructure, trust models, revocation, directories.

UNIT – III **9**

Message Authentication and Digital Signatures: Requirement of Authentication Functions, Message Authentication Codes, Hash and MAC Algorithms, MD2, MD4,MD5, SHA, HMAC, CMAC, Whirlpool, Address bases authentication, password based authentication, trusted intermediaries, digital Signatures, Digital Signature Standard.

UNIT – IV **9**

IP Security, Transport Layer Security: IP Sec, Authentication header, Encapsulating Security Payload, IKE, ISAKMP/IKE Encoding, Web Security Issues, Secure Sockets Layer, Transport Layer Security, Negotiating cipher suites, compression methods , encoding, HTTPS, Secure Shell.

UNIT – V **9**

Network Security Applications: Electronic Mail Security, Privacy enhanced mail, PGP, SMIME, Authorization and Access control, Firewalls, Intrusion Detection and Prevention Systems, Honeypots, honetnets, scanning and analysis tools, Antivirus Software, Virtual Private Network.

List of Exercises / Experiments :

1. Implement the following substitution and transposition techniques concepts
   a. Playfair Cipher
   b. Column Transformation
2. Implement Hill Cipher Technique
3. Implement the RSA Asymmetric key algorithm
4. Implement the Diffie Hellman Asymmetric key algorithm
5. Implement the Digital Signature standard algorithm
6. Setup a honey pot and monitor the honey pot on network (KF Sensor)

7. Demonstrate Intrusion Detection System (IDS) using any tool (snort or any other s/w)	
Lecture: 45, Practical: 30, Total: 75	
REFERENCES / MANUALS / SOFTWARES:	
1.	William Stallings, "Cryptography and Network Security Principles and Practices", 6th Edition, Prentice Hall, 2013.
2.	Behrouz A. Fourouzan, "Cryptography and Network Security", 2nd Edition, Tata McGraw-Hill, 2012.
3.	Charlie Kaufman, RadiaPeralman, Mike Speciner, "Network Security: Private communication in public world", 2nd Edition, Prentice Hall, 2002.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	identify the attacks against network infrastructure and the sources of attacks	Understanding (K2)
CO2:	evaluate the design principles of conventional encryption and public key encryption	Applying (K3)
CO3:	narrate the MAC and hashing techniques needed for authentication	Understanding (K2)
CO4:	identify the various types of security controls available to protect the network infrastructure	Understanding (K2)
CO5:	implement appropriate security controls to safeguard the network infrastructure	Applying (K3)
CO6:	practice the different types of symmetric key cryptographic algorithms	Applying (K3), Precision (S3)
CO7:	implement the various types asymmetric key cryptographic algorithms	Applying (K3), Precision (S3)
CO8:	demonstrate the different types of firewalls and intrusion detection system	Applying (K3), Precision (S3)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5
CO1	3		3	3	
CO2	3		3	3	
CO3	3		3	3	
CO4	3		3	3	
CO5	3		3	3	
CO6	3	2	3	3	1
CO7	3	2	3	3	1
CO8	3	2	3	3	1

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

18ESE01 SOLAR AND ENERGY STORAGE SYSTEM

L	T	P	Credit
3	0	0	3

Preamble	To understand and apply the process of PV systems. power point tracking and design of PV systems	
Prerequisites	Basics of Electronics	
UNIT – I		**9**
Introduction: Characteristics of sunlight – semiconductors and P-N junctions –behavior of solar cells – cell properties – PV cell interconnection.		
UNIT – II		**9**
Solar PV Modules and Arrays: Ratings of PV Module- Standard PV Module Parameters- Factors Affecting Electricity Generated by a Solar PV Module- Measuring Module Parameters- Connection of Modules in Series- Connection of Modules in Parallel Combination- Connection of Modules in Series and Parallel.		
UNIT – III		**9**
Batteries and Applications of Batteries in Solar PV Systems: Types of Batteries- Parameters of Batteries- Comparison of Various Rechargeable Batteries- Batteries for Photovoltaic (PV) Systems- Design of Lead-acid Batteries- Applications of Batteries in Solar PV Systems.		
UNIT – IV		**9**
Charge Controller, MPPT and Inverters: Power Converters and Their Efficiency- AC to DC Converters- DC to AC Converter (Inverters)- DC to DC Power Converters- Charge Controllers- Maximum Power Point Tracking (MPPT).		
UNIT – V		**9**
Solar PV System Design and Integration: Types of Solar PV Systems- Design Methodology for SPV System Applications: Case Studies: Solar Lighting-Solar Cooking-Solar Drying-Solar Desalination-Solar Furnaces.		
		Total: 45

REFERENCES :

1. Sukhatme S.P. and Nayak J.K., "Solar Energy", 4th Edition, Tata McGraw Hill, 2017.
2. Chetan Singh Solanki, "Solar Photovoltaic Technology and Systems, A Manual for Technicians, Trainers and Engineers", PHI Learning Pvt. Ltd., 2013.
3. Eduardo Lorenzo G. Araujo, "Solar electricity engineering of photovoltaic systems", Progensa,1994.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	infer the characteristics of sunlight and the role of semiconductors in solar cell	Understanding (K2)
CO2:	relate types and design of various PV interconnected systems	Applying (K3)
CO3:	apply the concepts of MPPT algorithm for PV module in Matlab	Applying (K3)
CO4:	choose system components of different PV applications	Applying (K3)
CO5:	infer on simple case study Solar Lighting - Solar Cooking - Solar Drying - Solar Desalination - Solar Furnaces	Understanding (K2)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1			2	2		
CO2			3	2		
CO3	2		3	2		
CO4	1		3	2		
CO5	2		2	2		2

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

18ESE02 SIGNAL AND IMAGE PROCESSING FOR EMBEDDED APPLICATIONS				
	L	**T**	**P**	**Credit**
	2	**0**	**2**	**3**

Preamble	To develop the image processing tools from scratch, rather than using any image processing library functions
Prerequisites	Signals and Systems

UNIT – I	**6**

Digital Image Fundamentals: Elements of digital image processing systems- Brightness- Contrast- Hue-saturation- Mach band effect -2D Image sampling- 2D Image transforms: DCT – KLT – Haar. Image Enhancement: Basic intensity transformations – Histogram equalization - Spatial filtering : Smoothing and sharpening Filters – Frequency domain filtering : Smoothing and sharpening filters – Homomorphic filters

UNIT – II	**6**

Morphological Image Processing: Erosion – Dilation – Duality – Opening – Closing – Hit or Miss Transformation– Basic Morphological Algorithms : Boundary Extraction- Hole filling – Extraction of connected components – Thinning – Thickening – Grayscale Morphology – Morphological smoothing – Morphological gradient – Tophat and bottom hat transformation

UNIT – III	**6**

Image Segmentation: Point, line and edge detection – Basics of intensity thresholding – Region based segmentation: Region growing - Region splitting and merging. Image Compression: Fundamentals: Types of redundancy – Huffmann – Run length coding – Arithmetic coding - Block Transform coding

UNIT – IV	**6**

Pattern Recognition: Patterns and Pattern classes – Representation of Pattern classes – Approaches to object recognition :Baye's Parametric classification – Template matching method – Structural Pattern Recognition: statistical and structural approaches

UNIT – V	**6**

Overview of Speech Processing: Speech Fundamentals: Articulatory Phonetics – Production and Classification of Speech Sounds; Acoustic Phonetics – acoustics of speech production; Short time Homomorphic Filtering of Speech; Linear Prediction (LP) analysis: Basis and development, LPC spectrum.

List of Exercises / Experiments :

1. Simulation of Basic operations on images and image enhancement algorithms
2. Simulation of morphological operations and algorithms
3. Simulation of simple edge detection and thresholding algorithms
4. Finger print Recognition
5. Face Recognition

Lecture:30, Practical:30, Total: 60

REFERENCES / MANUALS / SOFTWARES:

1. Gonzalez R.C. and Woods R.E., "Digital Image Processing", 4th Edition, Pearson Education, 2009.
2. Jayaraman S., Esakkirajan S. and Veerakumar T., "Digital Image Processing", 1st Edition, Tata McGraw-Hill, New Delhi, 2009.
3. Hayes H. Monson, "Statistical Digital Signal Processing and Modeling", John Wiley & Sons Inc., 1996.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	interpret the basic image processing spatial domain characteristics of digital images	Understanding (K2)
CO2:	apply Haar, DCT and KL Transforms to transform from spatial domain to other domains	Applying (K3)
CO3:	apply morphological operators and segmentation algorithms to extract the edges and regions of interest	Applying (K3)
CO4:	employ Huffmann, Arithmetic, Runlength and nblock transform coding techniques and compress the images	Applying (K3)
CO5:	examine the pattern recognition and speech processing approaches	Analyzing (K4)
CO6:	experiment basic image processing algorithms	Applying (K3), Manipulation (S2)
CO7:	apply edge detection and thresholding algorithms	Applying (K3), Manipulation (S2)
CO8:	use image processing technique for biometric authentication	Applying (K3), Precision (S3)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1			3	3		
CO2			3	2		
CO3	2		3	3		
CO4	2		3	3		
CO5	1		2	3		
CO6	1		3	2		
CO7	1		3	3		
CO8	2		3	3		2

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

18ESE03 QT CROSS COMPILING APPLICATION DEVELOPMENT					
		L	**T**	**P**	**Credit**
		3	**0**	**0**	**3**
Preamble	To know the basic concepts of Qt - single cross platform and to use C++ tool to design, develop, test, deploy programs for projects.				
Prerequisites	Basics of C++				
UNIT – I					**9**
Introduction to C++: Basic Concepts - Conditionals and Loops - Data Types, Arrays, Pointers – Functions - Classes and Objects - Inheritance and Polymorphism – sample programs.					
UNIT – II					**9**
Qt Installation and Compilation: Qt Framework on different platforms – sample application on current platform - Qt Quick access – QMessageBox -signals and slot - UI design – push button – line edit –label – style sheet.					
UNIT – III					**9**
Qt Platforms: Qt Android – configuration – linking – compiling - sample programs –link image – inbuilt resource - application development – Libraries .					
UNIT – IV					**9**
Internet of Things: Qtweb – QwebView - QNetworkAccessManager - collect and store sensor data - analyze and visualize data – sample programs.					
UNIT – V					**9**
Application Development: Design UI file – algorithm design – compile and debug – run application.					
					Total: 45
REFERENCES / MANUALS / SOFTWARES:					
1.	Stanley B. Lippman, Josee Lajoie, Barbara E. Moo, "C++ Primer", 4th Edition, Pearson Education, 2007.				
2.	Lee Zhi Eng, "Hands on GUI Programming with C++ and Qt5", 1st Edition, Packt Publishing Ltd., 2018.				
3.	Doc.qt.io/qt-5/index.html				

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	use class level C++ programs for simple applications.	Applying (K3)
CO2:	apply programming concepts in simple application for desktop.	Applying (K3)
CO3:	write android application programs.	Creating (K6)
CO4:	choose devices for Internet of things.	Applying (K3)
CO5:	develop basic application for end user.	Creating (K6)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1			3	2		
CO2			3	2		
CO3	2		3	2		1
CO4			3	1		
CO5	2		3	3	2	2

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

18ESE04 VERILOG HDL FOR EMBEDDED FPGA PROCESSOR				
	L	**T**	**P**	**Credit**
	3	**0**	**0**	**3**

Preamble	To understand the fundamentals of Verilog HDL programming and interfacing techniques for various Embededd FPGA processor.
Prerequisites	Digital Electronics

UNIT – I	**9**

Verilog Concepts: Introduction- Design flow- Design hierarchy- components of a simulation- Basic concepts- Data types - System tasks and compiler Directives-Modules and ports-test bench.

UNIT – II	**9**

Modeling with Verilog HDL: Overview of digital design using Verilog-HDL-Gate level Modeling-Dataflow Modeling-Behaviour Modeling-Tasks and Functions-Switch level modeling.

UNIT – III	**9**

Logic Synthesis with Verilog HDL: Verilog HDL Synthesis-Synthesis Design Flow-Verification of the gate level net list Modeling for logic synthesis-Example of sequential circuit synthesis.

UNIT – IV	**9**

Digital System Design: Design of a FSM: Mealy and Moore outputs, FSM representation, FSM code development and Design examples. Design of FSMD: Single RT operation, ASMD chart, Code development of an FSMD, Design examples.

UNIT – V	**9**

Embedded FPGA Processor and Interfacing: Overview of FPGA Device and EDA software- FPGA, Xilinx Spartan3 devices, Digilent S3 board, Development flow and Xilinx ISE Project Navigator. UART interface, Seven Segment Interface, Keyboard/Mouse Interface.

Total: 45

REFERENCES:

1. Samir Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", 2nd Edition, Pearson Education, New Delhi, 9th Impression, 2010.
2. Pong P. Chu, "FPGA Prototyping By Verilog Examples Xilinx Spartan-3 Version", 1st Edition, A John Wiley & Sons Publications, New Jersey, 2008.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	recall the Verilog programming concepts about data types, modules and test bench.	Remembering (K1)
CO2:	distinguish the gate level, data flow, behavioral and switch level modeling techniques of Verilog programming	Understanding (K2)
CO3:	design combinational and sequential circuits using Verilog programming	Creating (K6)
CO4:	design finite state machine circuits using Verilog programming	Creating (K6)
CO5:	interface peripherals with embedded Xilinx Spartan 3 FPGA processor	Applying (K3)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1			3	2		
CO2			3	2		
CO3	1		2	3		
CO4	1		2	3		
CO5	2		3	2		

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

18ESE05 MEDICAL IMAGING SYSTEMS

L	T	P	Credit
3	0	0	3

Preamble	To gain more knowledge on Image processing techniques and algorithms for the application of various Bio-medical Image analysis, detection and diagnosis.	
Prerequisites	Basics of Image Processing	
UNIT – I		**9**

Fundamentals of Medical Imaging: Introduction, Image Formation, Interaction of Electromagnetic Radiation With Matter in Medical Imaging.

UNIT – II		**9**

Image Preprocessing: Image enhancement – point operation, Histogram modeling, spatial operations, Transform operations, Image restoration – Image degradation model, Inverse and Weiner filtering. Image Compression –Spatial and Transform methods.

UNIT – III		**9**

Medical Image Reconstruction: Mathematical preliminaries and basic reconstruction methods, Image reconstruction in CT scanners, MRI, fMRI, Ultra sound imaging, 3D Ultra sound imaging, Nuclear imaging- Medicine Imaging Modalities- CT, MRI, fMRI, Ultra sound imaging, 3D Ultra sound imaging, Nuclear imaging, SPECT, PET, Molecular Imaging.

UNIT – IV		**9**

Image Analysis and Classification: Image segmentation- pixel based, edge based, region based segmentation. Image representation and analysis, Feature extraction and representation, Statistical, Shape, Texture, feature and image classification – Statistical, Rule based, Neural Network approaches.

UNIT – V		**9**

Image Registration and Visualization: Rigid body visualization, Principal axis registration, Interactive principal axis registration, Feature based registration, Elastic deformation based registration, Medical image fusion, Image visualization –2D display methods, 3D display methods, virtual reality based interactive visualization.

Total: 45

REFERENCES:

1. Atam P.Dhawan, "Medical Image Analysis", 2nd Edition, IEEE Press, 2011.
2. Rafael C. Gouzalez and Richard E. Woods, "Digital Image Processing", 3rd Edition, Pearson Education, 2016.
3. Jerry L. Prince and Jonathan Links, "Medical Imaging Signals and Systems", Pearson Education Inc., 2008.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	interpret medical image formation from Electromagnetic radiation and interpret the images for improving its quality using preprocessing techniques and reduction of noise in an image	Applying (K3)
CO2:	realize different modality of images from sensor	Understanding (K2)
CO3:	apply segmentation techniques to identify the edges and different regions of interest for a given image	Applying (K3)
CO4:	analyze the features of a given image	Analyzing (K4)
CO5:	apply registration process to perform image fusion and visualize them in 2D and 3D of a given multimodality images	Applying (K3)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1			3	3		
CO2			3	3		
CO3	1		3	2		
CO4	2		3	2		
CO5	1		3	2		

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

18ESE06 COMPUTER BASED INDUSTRIAL CONTROL					
		L	**T**	**P**	**Credit**
		3	**0**	**0**	**3**
Preamble	To know the need, levels different technologies in robotics and programming aspects of PLC for real time applications in industrial automation.				
Prerequisites	Microprocessors and Microcontrollers				
UNIT – I					**9**
Introduction: Automation in Production System, Principles and Strategies of Automation Basic Elements of an Automated System, Advanced Automation Functions, Levels of Automations.					
UNIT – II					**9**
Control Technologies in Automation: Industrial Control Systems, Process Industries Versus Discrete-Manufacturing Industries, Continuous Versus Discrete Control, sensors, actuators and other control system components.					
UNIT – III					**9**
Robotics in industrial Automation: Robot anatomy and Related Attributes, Robot control systems, End Effectors, Sensors in Robotics, Industrial Robot Applications ,Robot programming, Engineering analysis of Robots**.**					
UNIT – IV					**9**
PLC in industrial Automation: Introduction to PLC, Discrete Process Control: logic control- sequencing, ladder logic diagrams, Programmable Logic Controllers: components of the PLC-PLC operating cycle-additional capabilities of the PLC- Programming the PLC, Personal computers using soft logic.					
UNIT – V					**9**
Case Studies and Safety Measures: Industrial Control Applications: Cement, Thermal, Water Treatment, Steel Plants, Process Control plant, Textile and Dyeing industries, Industrial safety measures.					
					Total: 45
REFERENCES:					
1.	Groover M.P., "Automation, Production Systems and Computer Integrated Manufacturing", 5th Edition, Pearson Education, 2009.				
2.	Krishna Kant, "Computer Based Industrial Control", 2nd Edition, EEE-PHI, 2010.				
3.	Webb W. John and Reis A. Ronald, "Programmable Logic Controllers", 5th Edition, Prentice Hall Publications, 2006.				

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	identify the principles, elements and levels of integrated industrial automation system.	Understanding (K2)
CO2:	realize industrial control systems and analyze of continuous and discrete technologies with different sensors and actuators.	Understanding (K2)
CO3:	point out the anatomy, applications and programming methods of robotics for industrial automation	Understanding (K2)
CO4:	write programming for PLC based industrial application	Applying (K3)
CO5:	apply the industrial automation concepts for real-time applications and select the industrial safety measures	Applying (K3)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2		3	2		
CO2			2	3		
CO3			2	3		
CO4			3	2		
CO5	2		3	3	1	1

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

18VLE12 NATURE INSPIRED OPTIMIZATION TECHNIQUES

(Common to VLSI Design , Communication Systems, Embedded Systems, Computer Science and Engineering & Mechatronics branches)

L	T	P	Credit
3	0	0	3

Preamble	To acquaint and familiarize with different types of optimization techniques, solving optimization problems, implementing computational techniques, abstracting mathematical results and proofs etc.
Prerequisites	Linear algebra and Calculus

UNIT – I **9**

Introduction to Algorithms: Newton's Method – Optimization - Search for Optimality - No-Free-Lunch Theorems - Nature-Inspired Metaheuristics - Brief History of Metaheuristics. **Analysis of Algorithms:** Introduction - Analysis of Optimization Algorithms - Nature-Inspired Algorithms - Parameter Tuning and Parameter Control.

UNIT – II **9**

Simulated Annealing: Annealing and Boltzmann Distribution - Parameters - SA Algorithm - Unconstrained Optimization - Basic Convergence Properties - SA Behavior in Practice - Stochastic Tunneling. **Genetic Algorithms** : Introduction - Genetic Algorithms - Role of Genetic Operators - Choice of Parameters - GA Variants - Schema Theorem - Convergence Analysis

UNIT – III **9**

Particle Swarm Optimization: Swarm Intelligence - PSO Algorithm - Accelerated PSO – Implementation - Convergence Analysis - Binary PSO – Problems. **Cat Swarm Optimization:** Natural Process of the Cat Swarm - Optimization Algorithm – Flowchart - Performance of the CSO Algorithm.

UNIT – IV **9**

TLBO Algorithm: Introduction - Mapping a Classroom into the Teaching-Learning-Based optimization – Flowchart- Problems. **Cuckoo Search:** Cuckoo Life Style - Details of COA – flowchart - Cuckoos' Initial Residence Locations - Cuckoos' Egg Laying Approach - Cuckoos Immigration - Capabilities of COA. **Bat Algorithms:** Echolocation of Bats - Bat Algorithms – Implementation - Binary Bat Algorithms - Variants of the Bat Algorithm - Convergence Analysis.

UNIT – V **9**

Other Algorithms: Ant Algorithms - Bee-Inspired Algorithms - Harmony Search - Hybrid Algorithms.

Total: 45

REFERENCES:

1. Xin-She Yang, "Nature-Inspired Optimization Algorithms", 1st Edition, Elsevier, 2014.
2. Omid Bozorg-Haddad, "Advanced Optimization by Nature-Inspired Algorithms" Springer Volume 720, 2018.
3. Srikanta Patnaik, Xin-She Yang, Kazumi Nakamatsu, "Nature-Inspired Computing and Optimization Theory and Applications", Springer Series, 2017.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	infer the basic concepts of optimization techniques	Understanding (K2)
CO2:	identify the parameter which is to be optimized for an application	Analyzing (K4)
CO3:	analyze and develop mathematical model of different optimization algorithms	Analyzing (K4)
CO4:	select suitable optimization algorithm for a real time application	Applying (K3)
CO5:	recommend solutions, analyses, and limitations of models	Analyzing (K4)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	2	2	2	3
CO2			2	3	2	
CO3			2	3	2	
CO4			3	3	3	
CO5			2	3	2	

1 – Slight, 2 – Moderate, 3 – Substantial, BT – Bloom's Taxonomy

18CIE15 VIRTUAL INSTRUMENTATION FOR INDUSTRIAL APPLICATIONS

(Common to Control and Instrumentation Engineering, Embedded Systems, Applied Electronics & Power Electronics Drives branches)

L	T	P	Credit
3	0	0	3

Preamble	To impart knowledge about advanced tools in virtual instrumentation to develop new industrial applications
Prerequisites	Virtual Instrumentation

UNIT – I **9**

Graphical System Design Programming Concepts: G-Programming- debugging techniques-Loops: For loop, While Loop, Shift registers-Structures: Case Structure, Sequence Structure, Event Structure, Timed Structure-

UNIT – II **9**

Data Acquisition and Interfacing: Data Acquisition in LabVIEW-Hardware installation and configuration-DAQ components-DAQ signal Accessory-DAQ Assistant-DAQ Hardware-DAQ Software.

UNIT – III **9**

GSD Programming Toolkits: Signal Processing and Analysis-Control System Design and Simulation-Digital Filter Design-Spectral Measurements-Report generation-PID Control-Biomedical Startup kit.

UNIT – IV **9**

VI Applications Part I: Material Handling System -Fiber-Optic Component Inspection Using Integrated Vision and Motion Components-Internet-Ready Power Network Analyzer for Power Quality Measurements and Monitoring.

UNIT – V **9**

VI Applications Part II: Developing Remote Front Panel LabVIEW Applications- Using the Timed Loop to Write Multirate Applications in LabVIEW - Client–Server Applications in LabVIEW- Neural Networks for Measurement and Instrumentation in Virtual Environments.

Total: 45

REFERENCES:

1. Jovitha Jerome, "Virtual Instrumentation using LabVIEW", 3rd Edition, PHI Learning Pvt. Ltd., New Delhi, 2012.
2. Sumathi S., Surekha P., "LabVIEW based Advanced Instrumentation Systems", Springer Science & Business Media, 2007.
3. Sanjay Gupta, Joseph, John, "Virtual Instrumentation using LabVIEW", 2nd Edition, Tata McGraw Hill, 2010.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	apply structured programming concepts in developing VI programs and employ various debugging techniques	Applying (K3)
CO2:	interface hardware devices with software using DAQ system	Applying (K3)
CO3:	design, implement and analyze an application using different tools	Applying (K3)
CO4:	apply knowledge on various tools in practical works	Applying (K3)
CO5:	create virtual instruments for real time applications	Applying (K3)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		3	3		2
CO2	3		3	3		2
CO3	3		3	3		2
CO4	3		3	3		2
CO5	3		3	3		2

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

18MSE18 DESIGN AND ANALYSIS OF ALGORITHMS

(Common to Embedded Systems & Applied Electronics branches)

L	T	P	Credit
3	0	0	3

Preamble: To introduce the fundamental concepts of designing strategies, complexity analysis of algorithms, followed by problems on graph theory and sorting methods and also includes the basic concepts on complexity theory.

Prerequisites: C and Data Structures

UNIT – I **9**

Introduction: The Role of Algorithms in Computing – Growth of Functions – Analysis of Recursive and Non-recursive Functions – Lists – Heap Sort – Quick Sort – Sorting in Linear Time.

UNIT – II **9**

Advanced Data Structures: Binary Search Trees – Red-Black Trees – Augmenting Data Structures – Trees – Fibonacci Heaps

UNIT – III **9**

Algorithm Design Techniques: Dynamic Programming – Rod cutting – Matrix-chain multiplication – Elements of dynamic programming – Longest common subsequence – Optimal binary search trees. Greedy Algorithms: An activity-selection problem – Elements of the greedy strategy – Huffman codes – Matroids and greedy methods – A task-scheduling problem as a matroid Parallel Algorithms**:** Parallelism Introduction – The Pram Model – Simple parallel operations – Parallel searching, sorting, numerical algorithms – Parallel Graph algorithms

UNIT – IV **9**

Graph Algorithms: Elementary Graph Algorithms – Minimum Spanning Trees – Single Source Shortest Paths – All-Pairs Shortest Paths – Maximum Flow.

UNIT – V **9**

Non-Deterministic Algorithms: NP-Completeness: Polynomial Time verification – NP Completeness and Reducibility – NP Completeness Proofs – NP Complete Problems

Total: 45

REFERENCES:

1. Thomas H. Cormen, Charles E. Leiserson, Ronald L. Rivest and Clifford Stein, "Introduction to Algorithms", 3rd Edition, MIT Press, USA, 2009.
2. Jeffrey J. McConnell Canisius College, "Analysis of Algorithms: An Active Learning Approach", Jones and Bartlett Publishers, 2001.
3. Aho Alfred V., Hopcroft John E. and Ulllman Jeffrey D., "Data Structures and Algorithms", Pearson Education, New Delhi, 2002.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	design and implement elementary data structures	Creating (K6)
CO2:	design and implement advanced data structures	Creating (K6)
CO3:	choose appropriate algorithm design technique and solve problems	Applying (K3)
CO4:	implement graph algorithms	Applying (K3)
CO5:	analyze the time and space complexity of algorithms	Analyzing (K4)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1			2	3		
CO2			2	3		
CO3	2		3	2		
CO4	1		3	2		
CO5	2		2	3		

1 – Slight, 2 – Moderate, 3 – Substantial BT – Bloom's Taxonomy

18ESE07 DATA ANALYSIS FOR ENGINEERING

L	T	P	Credit
3	0	0	3

Preamble	To understand the analytics of big data process and visualization used in text and time series datasets.
Prerequisites	Number System

UNIT – I **9**

Data Analysis Process: Data, information, and knowledge - Nature of Data - Data Analysis Process: Problem Statement - Data Preparation - Data Exploration - Predictive Modeling -Visualization of Result- Quantitative vs Qualitative data analysis - Big Data: Sensors and Camera-Social Network Analysis.

UNIT – II **9**

Data Preprocessing and Formatting: Data Source - Data Scrubbing - Data Format - NumPy Basics: Arrays and Vectorized Computation- Data Loading, Storage, and File Formats - Data Cleaning and Preparation - Data Wrangling: Join, Combine and Reshape.

UNIT – III **9**

Data Load, Store and Visualizations: Retrieving, Processing, and Storing Data, Data Visualization: Basic matplotlib plots- Logarithmic plots- Scatter plots- Legends and annotations- Three-dimensional plots- Autocorrelation plots- Data-Driven Documents (D3).

UNIT – IV **9**

Text Data Analysis: Text Classification: Learning and classification- Bayesian classification- E-mail subject line tester- algorithm- Classifier accuracy.

UNIT – V **9**

Time series data analysis and working with SVM: Time series dataset: Components of a time series- Smoothing the time series, Multivariate dataset- Dimensionality reduction- support vector machine.

Total: 45

REFERENCES:

1. Hector Cuesta, "Practical Data Analysis -Transform-model-and-visualize-your-data-through-hands-on-projects-developed-in-open-source-tools", 2nd Edition, Packt Publisher, 2016.
2. Wes McKinney, "Python for Data Analysis: Data wrangling with Pandas, Numpy and I Python", 2nd Edition,O-Reilly,2017.
3. Ivan Idris, "Python Data Analysis", Packt Publishing, 2014.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	realize the data analysis process	Understanding (K2)
CO2:	manipulate preprocessing and formatting the given data using python libraries	Applying (K3)
CO3:	experiment the load, store and visualization of data using python libraries	Applying (K3)
CO4:	infer text and time series data using python libraries	Understanding (K2)
CO5:	summarize the concept of dimensional reduction and support vector analysis	Understanding (K2)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1			3	2		
CO2	1		3	2		
CO3			3	2		
CO4			3	2		
CO5	1	2	3	2		

1 – Slight, 2 – Moderate, 3 – Substantial, BT – Bloom's Taxonomy

18ESE08 RTOS FOR EMBEDDED SYSTEMS

L	T	P	Credit
2	0	2	3

Preamble	To provide a clear description of the concepts that underlie operating systems such as the ability to complete performance measurements at run-time, to direct the signal or send messages to tasks and to achieve pending on multiple kernel objects.
Prerequisites	Microprocessors

UNIT – I **6**

Introduction to Operating Systems: Function of OS –Computer system organization – Computer System Architecture - Operating system Operations – Process management – Memory Management – Protection and Security - **System Structures:** Operating system Services – User and Operating system Interface – System calls – Types of System Calls – Operating systems design and Implementation – Operating system Structure.

UNIT – II **6**

Real Time Systems: Overview-System Characteristics-Features of Real time kernels-Implementing real time operating systems - RTOS Concepts: Foreground/Background systems – Real time kernels – RTOS – Scheduling: Preemptive scheduling – Scheduling Points - Round robin scheduling – scheduling Internals

UNIT – III **6**

µC/OS-III: Introduction - µC/OS-III Features - Goals of µC/OS-III – Directories and Files – Critical Sections- Tasks –Task States – Task Scheduling – Idle Task – Statistics Task – Interrupts Under µC/OS-III – Clock Tick - µC/OS-III Initialization. Task Management: Assigning Task Priorities-Determining the size of stack-Detecting Task stack overflows-Task management services-Task Management Internals-Internal Tasks - Time Management.

UNIT – IV **6**

Resource Management: Disable/Enable Interrupts - Lock/Unlock- Semaphores- Mutex semaphore – Deadlock – Synchronization: Semaphore – Task Semaphore – Event Flags -Synchronizing multiple tasks. **Message Passing:** Messages – Messages Queues – Task Message Queue – bilateral rendezvous – Flow control – using message queues – clients and servers – message queue Internals.

UNIT – V **6**

Memory Management: Creating a memory Partition- getting a Memory Block from partition– Returning a Memory Block to a partition-using memory partitions- Porting µC/OS-III: µC/CPU-µC/OS-III Port- Board support Package - Case study of coding for an Automatic Chocolate Vending Machine using MUCOS RTOS.

List of Exercises / Experiments:

1. Simulation of Task Creation, Dynamic Priority, Time Management
2. Simulation of Binary Semaphore and Counting Semaphore
3. Simulation of Mutex and Message Queue
4. Simulation of Memory Partition Creation
5. Simulation of Memory Block Allocation

Lecture: 30, Practical: 30, Total: 60

REFERENCES:

1. Silberschatz A., Galvin P.B., Gagne G., "Operating System Concepts", 8th Edition, Wiley, 2009.
2. Jean J. Labrosse, "µC/OS - III The Real Time Kernel User's 3.6.01 Manual", Micrium Press, 2014.
3. Raj Kamal, "Embedded Systems: Architecture, Programming and Design", 2nd Edition, Tata McGraw Hill Education, 2008.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	define the characteristics of real time systems	Remembering (K1)
CO2:	realize the concepts of scheduling employed in RTOS	Applying (K3)
CO3:	apply task creation, priority assignment, and time management services provided by μC/OS – III	Applying (K3)
CO4:	apply semaphore, mutex, and message queue services in a task	Applying (K3)
CO5:	demonstrate memory partitions and allocations techniques used in RTOS and porting μC/OS - III to a different architecture	Applying (K3)
CO6:	make use task creation, priority, time management and semaphore concepts of RTOS for different applications	Applying (K3), Manipulation (S2)
CO7:	implement message queue for inter process communication	Applying (K3), Manipulation (S2)
CO8:	carryout memory block allocation for an application	Applying (K3), Manipulation (S2)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1			3	2		
CO2			3	2		
CO3	2		3	2		
CO4	2		3	2		
CO5	2		3	2		2
CO6	1		3	2		
CO7			3	2		
CO8			3	2		

1 – Slight, 2 – Moderate, 3 – Substantial, BT – Bloom's Taxonomy

18ESE09 SYSTEM ON CHIP

L	T	P	Credit
3	0	0	3

Preamble	To know the architecture of embedded processor like ARM processor and to study different operating systems
Prerequisites	Microprocessors

UNIT – I **9**

Introduction to System on Chip Design: Processor architecture and organization ,Abstraction in hardware design, MU0 - a simple processor, Instruction set design , Processor design trade-offs, The Reduced Instruction Set Computer, Design for low power consumption, ARM architecture.

UNIT – II **9**

ARM Organization and Implementation: 3-stage pipeline ARM organization, 5-stage pipeline ARM organization, ARM instruction execution and implementation, coprocessor interface, The ARM instruction set and programming.

UNIT – III **9**

ARM Processor Cores and Memory Hierarchy: ARM7TDMI, ARM8, and ARM9TDMI ARM10TDMI - Memory size and speed, On-chip memory, Caches, Cache design - an example, Memory management.

UNIT – IV **9**

Architectural Support for Operating Systems: An introduction to operating systems, The ARM system control coprocessor,CP15 protection unit registers, ARM protection unit, CP15 MMU registers, ARM MMU architecture, Synchronization, Context switching, Input/output.

UNIT – V **9**

Embedded ARM Applications: The VLSI Ruby II Advanced Communication Processor, The VLSI ISDN Subscriber Processor, The Ericsson-VLSI Bluetooth Baseband Controller, The ARM7500 and ARM7500FE, case study on The DRACO telecommunications controller.

Total: 45

REFERENCES:

1. Steve Furber, "ARM System-on-Chip Architecture", 2nd Edition, Pearson, 2015.
2. Andrew Sloss, Dominic Symes, Chris Wright, "ARM System Developer's Guide: Designing and Optimizing System Software (The Morgan Kaufmann Series in Computer Architecture and Design)", 1st Edition, Elsevier Publications, 2011.
3. Yifeng Zhu, "Embedded Systems with ARM Cortex-M Microcontrollers in Assembly Language and C", 3rd Edition, E-Man Press LLC, 2017.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	identify the basic design of system on chip with ARM architecture as a reference	Understanding (K2)
CO2:	know the 3-line and 5-line pipelining concept of ARM organisation and programming with instruction set	Understanding (K2)
CO3:	realize the memory hierarchy and design of different ARM7, ARM8, ARM9 and ARM10 processor cores	Applying (K3)
CO4:	realize the concept of ARM operating systems, ARM protection unit and MMU.	Applying (K3)
CO5:	apply the system on chip concept for different embedded applications such as ISDN, Bluetooth and DRACO telecommunication controller	Applying (K3)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1			3	2		
CO2			3	2		
CO3	2		3	2		
CO4	2		3	2		
CO5	3		3	2		2

1 – Slight, 2 – Moderate, 3 – Substantial, BT – Bloom's Taxonomy

18ESE10 DESIGN OF EMBEDDED CONTROL SYSTEM

L	T	P	Credit
3	0	0	3

Preamble	To introduce the basic concepts of control systems and its embedded implementation.
Prerequisites	Microcontroller

UNIT – I **9**

Control System Basics: Z-transforms – performance requirements - block diagrams - analysis and design - sampling theory – difference equations.

UNIT – II **9**

Control System Implementation: Discretization method – Fixed point mathematics – Nonlinear controller elements – Gain scheduling – Controller implementation and testing in Embedded Systems - a case study of robotic control system.

UNIT – III **9**

Control System Testing: Software implications - Controller implementation and testing in embedded systems - Measuring frequency response.

UNIT – IV **9**

Input Devices: Keyboard basics - Keyboard scanning algorithm - Character LCD modules - LCD module display Configuration - Time-of-day clock - Timer manager - Interrupts - Interrupt service routines - Interrupt-driven pulse width modulation. Triangle waves analog vs. digital values - Auto port detect - Capturing analog information in the timer interrupt service routine - Automatic, multiple channel analog to digital data acquisition.

UNIT – V **9**

Output Devices and Sensors: H Bridge – relay drives - DC/ Stepper Motor control – optical devices. Linear and angular displacement sensors: resistance sensor – induction displacement sensor – digital optical displacement sensor – pneumatic sensors. Speed and flow rate sensors: electromagnetic sensors – fluid flow sensor – thermal flow sensor. Force sensors: piezoelectric sensors – strain gauge sensor – magnetic flux sensor – inductive pressure sensor – capacitive pressure sensor. Temperature sensors: electrical – thermal expansion – optical Case Study- Examples for sensor, actuator, control circuits with applications.

Total: 45

REFERENCES:

1. Jim Ledin, "Embedded control systems in C/C++", CMP Books, 2004.
2. TimWiscott, "Applied control for embedded systems", Elsevier Publications, 2006.
3. Jean J. Labrosse, "Embedded Systems Building Blocks: Completeand Ready-To-Use Modules in C", The Publisher, Paul Temme, 2011.
4. Lewin A.R.W. Edwards, "Open source robotics and process control cookbook", Elsevier Publications, 2005.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	identify the basics of control systems	Understanding (K2)
CO2:	implement control theory in embedded systems	Applying (K3)
CO3:	appraise the concept of control system in testing	Understanding (K2)
CO4:	apply the concept in the applications using control systems	Applying (K3)
CO5:	infer the input and output devices used in control systems	Understanding (K2)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1			2	2		
CO2	1		3	2		
CO3			1	2		
CO4	1		3	2		
CO5			2	2		

1 – Slight, 2 – Moderate, 3 – Substantial , BT – Bloom's Taxonomy

18ESE11 MULTICORE PROCESSOR AND COMPUTING

L	T	P	Credit
3	0	0	3

Preamble	To know the basic knowledge about multiprocessor, multicomputer systems and advanced processor technology in parallel processors
Prerequisites	Computer Architecture

UNIT – I **9**

Multi-Core Processors: Single core to Multi-core architectures – SIMD and MIMD systems – Interconnection networks - Symmetric and Distributed Shared Memory Architectures – Cache coherence - Performance Issues – Parallel program design.

UNIT – II **9**

Parallel Program Challenges: Performance – Scalability – Synchronization and data sharing – Data races – Synchronization primitives (mutexes, locks, semaphores, barriers) – deadlocks and live locks – communication between threads (condition variables, signals, message queues and pipes).

UNIT – III **9**

Shared Memory Programming with OpenMP: OpenMP Execution Model – Memory Model – OpenMP Directives – Work - sharing Constructs - Library functions – Handling Data and Functional Parallelism – Handling Loops - Performance Considerations.

UNIT – IV **9**

Distributed Memory Programming With MPI: MPI program execution – MPI constructs – libraries – MPI send and receive – Point-to-point and Collective communication – MPI derived data types – Performance evaluation.

UNIT – V **9**

Parallel Program Development: Case studies – n - Body solvers – Tree Search – OpenMP and MPI implementations and comparison.

Total: 45

REFERENCES:

1. Peter S. Pacheco, "An Introduction to Parallel Programming", Morgan - Kauffman/Elsevier, 2011.
2. Michael J. Quinn, "Parallel programming in C with MPI and OpenMP", 1st Edition, Tata McGraw Hill, 2003.
3. Shameem Akhter and Jason Roberts, "Multi-core Programming", Intel Press, 2006.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	interpret the operations of multiprocessor and multicomputer systems	Understanding (K2)
CO2:	describe the advanced processor technology, pipelining and scalable architectures	Understanding (K2)
CO3:	examine shared memory programming using OpenMP	Analyzing (K4)
CO4:	examine distributed memory programming with MPI	Analyzing (K4)
CO5:	implement parallel programming OpenMP and MPI	Applying (K3)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1			3	3		
CO2			3	2		
CO3			3	2		
CO4			2	3		
CO5			3	3		

1 – Slight, 2 – Moderate, 3 – Substantial, BT – Bloom's Taxonomy

18ESE12 PROGRAMMING INTERNET OF THINGS

L	T	P	Credit
3	0	0	3

Preamble	To learn the fundamentals of this emerging technology and to design of smart objects that provides collaboration and ubiquitous services.
Prerequisites	Microcontroller

UNIT – I **9**

IoT Architecture: IoT Architecture-State of the Art – Introduction, IoT Reference architecture, Functional View, Information View. Real-World Design Constraints- Introduction, Technical Design constraints-IOT Communication Models-Communication API's-IOT Enabling Technologies.

UNIT – II **9**

IoT Levels, M2M and System Management: IoT Levels1 to 6—M2M-Difference between IoT and M2M – SDN and NFV-Need of IoT system Management- with NETCONF and YANG, IoT Design Methodology.

UNIT – III **9**

Interoperability in IoT, Introduction to Programming Python: Data types – Data structures – Control flow – Functions – Modules – Packages – File Handling – Date and timeoperation – Classes – Python packages of IoT. IoT Physical Design: Basic building blocks – Raspberry Pi – Linux on Raspberry Pi – Interfaces(LED and Switch) – Programming on Raspberry Pi with Python

UNIT – IV **9**

Data Analytics and Web Framework: Data Analytics for IOT: Apache Hadoop-Map Reduce Models-Case Study : Batch Data Analysis and Real Time Data Analysis. Web Application Framework: Django,-Django Architecture-starting Development with Django.

UNIT – V **9**

Preparing IoT Projects: Raspberry Pi for Project Development: Raspberry Pi platform – GPIO – Establishment and setting of Raspberry Pi software – LAMP Installation– Home temperature monitoring system – Webcam and Raspberry Pi camera project.

Total: 45

REFERENCES:

1. Jan Holler, Vtasies Tsiatsis, "From machine to machine Internet of Things: Introductin to a new age of Intelligence", 1st Edition, Elsevier Publication, 2014.
2. Arshdeep Bahga, Vijay Madisetti, "Internet of Things: A Hands-On Approach", 1st Edition, 2014.
3. Donald Norris, "The Internet of Things: Do-It-Yourself at Home Projects for Arduino, Raspberry Pi and BeagleBone Black", 1st Edition, McGraw Hill, 2015.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	compare the IoT physical and logical architecture and its enabling technologies	Understanding (K2)
CO2:	interpret different IoT levels and networking methodologies	Understanding (K2)
CO3:	implement IoT programming concepts using python and its open source tools	Applying (K3)
CO4:	analyze the collected data based on data analytics tool - Hadoop, Django	Analyzing (K4)
CO5:	design and integrate projects using Raspberry Pi with temperature sensor, webcam	Creating (K6)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1			2	3		
CO2			2	3		
CO3	2		3	2		
CO4	2		2	3		
CO5	2	2	3	3	3	2

1 – Slight, 2 – Moderate, 3 – Substantial, BT – Bloom's Taxonomy

18ESE13 SINGLE BOARD COMPUTER

L	T	P	Credit
2	0	2	3

Preamble	To develop a basic knowledge in working with single board computer for multifunctional tasks like IoT, Image analysis for research applications.
Prerequisites	Digital Electronics, Microprocessor and Microcontroller

UNIT – I **6**

Introduction to SBC and Linux Basics: Types of single board computer - Linux file system - text editors - accessing files - power supply unit - preparation of boot SD card - configuration - networking with Host computer - terminal access.

UNIT – II **6**

Python Programming and Sensor Interfacing: Pin diagram - GPIO access - LED & Switch - Timers - external circuit interfacing - UART - sensor interfacing.

UNIT – III **6**

Peripheral Control: Interfacing touch screen - ADC, DAC and, Motor - DC Motor Control using PWM Relay and Stepper Motor interfacing.

UNIT – IV **6**

Internet of Things: Open API's for Internet of Things - collect and store sensor data - analyze and visualize data - control peripheral device.

UNIT – V **6**

Image Processing in SBC: Introduction to OPENCV - reading and writing images - create image - draw - conversion - merge - video processing - real-time image processing in SBC.

Lecture:30, Practical:30, Total: 60

List of Experiments:

1. Development of bootable OS and Initialize the setup of SBC using Raspberry Pi
2. Interfacing of GPIO for I/O devices in Raspberry Pi
3. Interfacing of digital sensors with Raspberry Pi
4. Development of Simple IoT Application
5. Mini Project - interfacing of sensors data through IOT

REFERENCES:

1. Eben Upton,Gareth Halfacree, “Raspberry Pi User Guide”, 4th Edition, Wiley, 2016.
2. https://www.raspberrypi.org/documentation
3. Joe Minichino, Joseph Howse, “Learning OpenCV 3 Computer Vision with Python”, 2nd Edition, Packt Publishing Ltd., 2015.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	employ programming concepts to manipulate ports and peripherals of SBC	Applying (K3)
CO2:	implement program for real time applications using SBC	Applying (K3)
CO3:	apply python programming language for internal and external peripherals	Applying (K3)
CO4:	choose devices for Internet of things	Understanding (K2)
CO5:	apply image processing for real time applications	Applying (K3)
CO6:	use different packages of python language for GPIO access	Applying (K3), Manipulation (S2)
CO7:	experiment with digital sensors using Raspberry Pi	Applying (K3), Manipulation (S2)
CO8:	develop a project to process the image and transfer the data through IOT	Applying (K3), Precision (S3)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1			3	2		
CO2	2		3	2		2
CO3			3	2		
CO4			3	3		
CO5	2		3	2		1
CO6			3	3		
CO7	2		3	3		
CO8	2		3	3		1

1 – Slight, 2 – Moderate, 3 – Substantial, BT – Bloom's Taxonomy