KONGU ENGINEERING COLLEGE
PERUNDURAI ERODE – 638 060
(Autonomous)

VISION

To be a centre of excellence for development and dissemination of knowledge in Applied Sciences, Technology, Engineering and Management for the Nation and beyond.

MISSION

We are committed to value based Education, Research and Consultancy in Engineering and Management and to bring out technically competent, ethically strong and quality professionals to keep our Nation ahead in the competitive knowledge intensive world.

QUALITY POLICY

We are committed to

- Provide value based quality education for the development of students as competent and responsible citizens.
- Contribute to the nation and beyond through research and development
- Continuously improve our services

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VISION

To be a centre of excellence for development and dissemination of knowledge in Electronics and Communication Engineering for the Nation and beyond

MISSION

Department of Electronics and Communication Engineering is committed to:

MS1: To impart industry and research based quality education for developing value based electronics and communication engineers

MS2: To enrich the academic activities by continual improvement in the teaching learning process

MS3: To infuse confidence in the minds of students to develop as entrepreneurs

MS4: To develop expertise for consultancy activities by providing thrust for Industry Institute Interaction

MS5: To endeavour for constant upgradation of technical expertise for producing competent professionals to cater to the needs of the society and to meet the global challenges

2018 REGULATIONS

PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

Graduates of M.E.(VLSI Design) will

PEO1: Succeed in industry and research by applying knowledge of modeling, design and fabrication techniques of Integrated Circuits

PEO2: Identify, design and analyze solutions to solve real world problems in VLSI design

PEO3: Demonstrate soft skills , professional and ethical values and aptitude for life long learning needed for a successful professional career

MAPPING OF MISSION STATEMENTS (MS) WITH PEOs

MS\PEO	PEO1	PEO2	PEO3
MS1	3	3	3
MS2	2	3	2
MS3	3	3	3
MS4	2	3	1
MS5	3	3	3

1 – Slight, 2 – Moderate, 3 – Substantial

PROGRAM OUTCOMES (POs)	
M.E(VLSI Design) Graduates will be able to:	
PO1:	Independently carry out research/investigation and development work to solve practical problems
PO2 :	Write and present a substantial technical report/document
PO3:	Demonstrate a degree of mastery over the areas of VLSI Systems, IC fabrication, design, testing, verification and prototype development focusing on applications
PO4 :	Integrate multiple sub-systems to develop System On Chip and optimize its performance
PO5:	Identify and apply appropriate Electronic Design Automation (EDA) tool to create innovative products/ systems to solve real world problems in VLSI domain
PO6:	Apply appropriate managerial and technical skills in the domain of VLSI design incorporating safety and sustainability to become a successful Professional / entrepreneur through lifelong learning

MAPPING OF PEOs WITH POs AND PSOs

PEO\PO	PO1	PO2	PO3	PO4	PO5	PO6
PEO1	3	3	3	3	3	2
PEO2	3	1	3	3	3	2
PEO3	3	1	3	3	3	3

1 – Slight, 2 – Moderate, 3 – Substantial

CURRICULUM BREAKDOWN STRUCTURE UNDER REGULATION 2018

Curriculum Breakdown Structure(CBS)	Curriculum Content (% of total number of credits of the program)	Total number of contact hours	Total number of credits
Program Core(PC)	41.67	450	30
Program Electives(PE)	25	270	18
Humanities and Social Sciences and Management Studies(HSMS)	5.56	60	4
Project(s)/Internships(PR)/Others	27.7	300	20
Total			**72**

KEC R2018: SCHEDULING OF COURSES – ME (VLSI Design)

Semester	Theory/ Theory cum Practical / Practical							Internship & Projects	Online/ VACs	Special Courses	Credits
	1	2	3	4	5	6	7	8	10	11	
I	Applied Mathematics for Electronic Engineers HSMS-1 (3-1-0-4)	Digital System For IC Design Pc-1 (3-1-0-4)	Device Modeling Pc-2 (3-0-0-3)	Testing of VLSI Circuits Pc-3 (3-1-0-4)	VLSI Design Techniques PC-4 (3-0-2-4)	HDL for IC Design PC-5 (3-0-2-4)					23
II	Analog IC Design PC-6 (3-0-2-4)	Application Specific Integrated Circuits PC-7 (3-0-2-4)	VLSI Signal Processing PC-8 (3-0-0-3)	Professional Elective I PE-1 (3-0-0-3)	Professional Elective II PE-2 (3-0-0-3)	Professional Elective III PE-3 (3-0-0-3)		Mini Project PR-1 (0-0-4-2)			22
III	Professional Elective I PE-4 (3-0-0-3)	Professional Elective II PE-5 (3-0-0-3)	Professional Elective III PE-6 (3-0-0-3)					Project work Phase – I PR-2 (0-0-12-6)		Audit Course (2-0-0-0)	15
IV								Project work Phase – II PR-2 (0-0-24-12)			12

Total Credits: 72

KONGU ENGINEERING COLLEGE, PERUNDURAI, ERODE - 638 060
(Autonomous)

M.E. DEGREE IN VLSI DESIGN

CURRICULUM

(For the candidates admitted from academic year 2018-19 onwards)

SEMESTER – I

Course Code	Course Title	Hours / Week			Credit	Maximum Marks			CBS
		L	T	P		CA	ESE	Total	
	Theory/Theory with Practical								
18AMT13	Applied Mathematics for Electronics Engineers	3	1	0	4	50	50	100	HS
18VLT11	Digital System For IC Design	3	1	0	4	50	50	100	PC
18VLT12	Device Modeling	3	0	0	3	50	50	100	PC
18VLT13	Testing of VLSI Circuits	3	1	0	4	50	50	100	PC
18VLC11	VLSI Design Techniques	3	0	2	4	50	50	100	PC
18VLC12	HDL for IC Design	3	0	2	4	50	50	100	PC
	Total				**23**				

CA – Continuous Assessment, ESE – End Semester Examination, CBS – Curriculum Breakdown Structure

KONGU ENGINEERING COLLEGE, PERUNDURAI, ERODE – 638 060
(Autonomous)

M.E. DEGREE IN VLSI DESIGN

CURRICULUM

(For the candidates admitted from academic year 2018-19 onwards)

SEMESTER – II

Course Code	Course Title	Hours / Week			Credit	Maximum Marks			CBS
		L	T	P		CA	ESE	Total	
	Theory/Theory with Practical								
18VLC21	Analog Integrated Circuit Design	3	0	2	4	50	50	100	PC
18VLC22	Application Specific Integrated Circuits	3	0	2	4	50	50	100	PC
18VLT21	VLSI Signal Processing	3	0	0	3	50	50	100	PC
	Elective - I	3	0	0	3	50	50	100	PE
	Elective - II	3	0	0	3	50	50	100	PE
	Elective - III	3	0	0	3	50	50	100	PE
	Practical								
18VLP21	Mini Project	0	0	4	2	100	0	100	PR
	Total				**22**				

CA – Continuous Assessment, ESE – End Semester Examination, CBS – Curriculum Breakdown Structure

KONGU ENGINEERING COLLEGE, PERUNDURAI, ERODE – 638 060
(Autonomous)

M.E. DEGREE IN VLSI DESIGN

CURRICULUM

(For the candidates admitted from academic year 2018-19 onwards)

SEMESTER – III

Course Code	Course Title	Hours / Week			Credit	Maximum Marks			CBS
		L	T	P		CA	ESE	Total	
	Theory/Theory with Practical								
	Elective - IV	3	0	0	3	50	50	100	PE
	Elective - V	3	0	0	3	50	50	100	PE
	Elective - VI	3	0	0	3	50	50	100	PE
	Practical								
18VLP31	Project Work Phase I	0	0	12	6	50	50	100	PR
	Total				**15**				

CA – Continuous Assessment, ESE – End Semester Examination, CBS – Curriculum Breakdown Structure

KONGU ENGINEERING COLLEGE, PERUNDURAI, ERODE – 638 060
(Autonomous)

M.E. DEGREE IN VLSI DESIGN

CURRICULUM

(For the candidates admitted from academic year 2018-19 onwards)

SEMESTER – IV

Course Code	Course Title	Hours / Week			Credit	Maximum Marks			CBS
		L	T	P		CA	ESE	Total	
	Practical								
18VLP41	Project Work Phase II	0	0	24	12	50	50	100	PR
	Total				**12**				

CA – Continuous Assessment, ESE – End Semester Examination, CBS – Curriculum Breakdown Structure

Total Credits: 72

LIST OF PROFESSIONAL ELECTIVES						
Course Code	**Course Title**	**Hours/Week**			**Credit**	**CBS**
		L	**T**	**P**		
SEMESTER II						
18COE04	Electromagnetic Interference and Compatibility	3	0	0	3	PE
18COE09	DSP Processor Architecture and Programming	2	0	2	3	PE
18VLE01	Computer Aided Design of VLSI Circuits	2	1	0	3	PE
18VLE02	Design of Semiconductor Memories	3	0	0	3	PE
18VLE03	Low Power VLSI Design	3	1	0	4	PE
18VLE04	Reconfigurable Architectures For VLSI	3	0	0	3	PE
18VLE05	Mixed Signal VLSI Design	3	0	0	3	PE
18VLE06	Supervised Machine Learning Algorithms	3	0	0	3	PE
18VLE07	VLSI for Biomedical Applications	3	0	0	3	PE
18VLE08	VLSI Technology	3	0	0	3	PE
SEMESTER III						
18MME13	MEMS Design	3	0	0	3	PE
18MIE14	Quantum Information and Computing	3	0	0	3	PE
18VLE09	Hardware Software Co-Design	3	0	0	3	PE
18VLE10	Intellectual Property Based VLSI Design	3	0	0	3	PE
18VLE11	Nanoelectronics	3	0	0	3	PE
18VLE12	Nature Inspired Optimization Techniques	3	0	0	3	PE
18VLE13	Network on Chip	3	0	0	3	PE
18VLE14	Genetic Algorithms for VLSI Circuits	3	0	0	3	PE
18VLE15	RF VLSI Design	3	0	0	3	PE
18VLE16	VLSI for Wireless Communication	3	0	0	3	PE

18AMT13 APPLIED MATHEMATICS FOR ELECTRONICS ENGINEERS

(Common to VLSI Design, Communication Systems and Embedded Systems Branches)

L	T	P	Credit
3	1	0	4

Preamble	This course will demonstrate various analytical skills in applied mathematics and use extensive mathematical tools such as linear programming, graph and queuing theory with the tactics of problem solving and logical thinking applicable in electronics engineering.
Prerequisites	Vectors and Probability

UNIT – I **9**

Vector Spaces: Definition – Subspaces – Linear dependence and independence – Basis and dimension – Row space, Column space and Null Space – Rank and nullity.

UNIT – II **9**

Linear Programming: Mathematical Formulation of LPP – Basic definitions – Solutions of LPP: Graphical method – Simplex method – Transportation Model – Mathematical Formulation - Initial Basic Feasible Solution: North west corner rule – Vogel's approximation method – Optimum solution by MODI method – Assignment Model – Mathematical Formulation – Hungarian algorithm.

UNIT – III **9**

Non-Linear Programming: Formulation of non–linear programming problem – Constrained optimization with equality constraints – Constrained optimization with inequality constraints – Graphical method of non–linear programming problem involving only two variables.

UNIT – IV **9**

Graph Theory: Introduction of graphs – Isomorphism – Subgraphs – Walks, paths and circuits – Connected graphs – Eulerian Graphs – Hamiltonian Paths and circuits – Digraph – Adjacency matrix and incidence matrix of graphs – Applications: Shortest path algorithms – Dijkstra's algorithm – Warshall's algorithm – Trees – Properties of trees – Spanning trees – Applications of trees: Minimal spanning trees – Prim's Algorithm – Kruskal's algorithm.

UNIT – V **9**

Queuing Theory: Markovian queues – Single and Multi-server Models – Little's formula – Non- Markovian Queues – Pollaczek Khintchine Formula.

Lecture:45, Tutorial:15, Total: 60

REFERENCES:

1. Howard Anton, "Elementary Linear Algebra", 10th Edition, John Wiley & Sons, 2010.
2. Kanti Swarup, Gupta P.K. and Man Mohan, "Operations Research", S. Chand & Co., 1997.
3. Bondy J.A. and Murthy, USR, "Graph Theory and Applications", Mc Millan Press Ltd., 1982.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	demonstrate accurate and efficient use of advanced algebraic techniques	Understanding (K2)
CO2:	formulate and solve linear programming problems that appear in electronics engineering	Evaluating (K5)
CO3:	use non-linear programming concepts in real life situations	Applying (K3)
CO4:	apply graph theoretic algorithms in design of systems	Applying (K3)
CO5:	analyze the characteristics of various queuing models	Analyzing (K4)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	2	2	2	3
CO2			1	2	1	
CO3			3	3	3	
CO4			3	3	3	
CO5			2	3	2	

1 – Slight, 2 – Moderate, 3 – Substantial, BT – Bloom's Taxonomy

18VLT11 DIGITAL SYSTEM FOR IC DESIGN

L	T	P	Credit
3	1	0	4

Preamble	To design and analyze synchronous, asynchronous digital circuits and to introduce ASM and the architectures of PLD
Prerequisites	Digital Electronics

UNIT – I **9**

Synchronous Sequential Circuit Design: Analysis of Clocked Synchronous Sequential Networks (CSSN) - Modeling of CSSN - State table Reduction - Stable Assignment - Complete Design of CSSN - Design of Iterative Circuits

UNIT – II **9**

Algorithmic State Machine (ASM): ASM - ASM Chart - Synchronous Sequential Network Design Using ASM Charts - State Assignment - ASM Tables - ASM Realization - Asynchronous Inputs.

UNIT – III **9**

Asynchronous Circuit Design: Analysis of Asynchronous Sequential Circuit (ASC) - Flow Table Reduction - Races in ASC - State Assignment - Problem and the Transition Table - Design of ASC - Static and Dynamic Hazards - Essential Hazards

UNIT – IV **9**

Programming Logic Arrays: PLA minimization - Essential Prime Cube theorem - PLA folding - Foldable compatibility matrix - The Compact Algorithm. Practical PLA's - Data Synchronizers - Designing Vending Machine Controller - Mixed Operating Mode Asynchronous Circuits

UNIT – V **9**

Programmable Devices: Programmable Logic Devices - Designing a Synchronous Sequential Circuit using a PAL - Realization State machine using PLD - Complex Programmable Logic Devices (CPLDs) - FPGA - Actel ACT.

Lecture: 45, Tutorial: 15, Total: 60

REFERENCES:

1. Givone Donald G., "Digital Principles and Design", Tata McGraw-Hill, New Delhi, 2002.
2. Biswas Nripendra N., "Logic Design Theory", Prentice Hall of India, New Delhi, 2001.
3. Yarbrough John M., "Digital Logic Applications and Design", Thomson Learning, Singapore, 2001.
4. Roth Charles H., "Fundamentals of Logic Design", Thomson Learning, Singapore, 2005.
5. Ming-Bo Lin, "Digital System Design and Practices: Using Verilog HDL and FPGAs", Wiley Publisher, New York, 2008.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	design clocked synchronous sequential circuits using state table reduction and assignment	Applying (K3)
CO2:	realize the algorithmic state machine using state tables, charts and state assignment	Applying (K3)
CO3:	analyze the asynchronous sequential circuit using flow table reduction and find the hazards in circuits	Analyzing (K4)
CO4:	simplify the circuits using Programmable logic array, essential cube theorem and compact algorithm	Applying (K3)
CO5:	design the synchronous sequential circuits using Programmable Logic Device, Programmable Array Logic and CPLD	Creating (K6)

Mapping of COs with Pos

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1			3	3	3	
CO2			3	3	3	
CO3			2	3	2	
CO4			3	3	3	
CO5				1		

1 – Slight, 2 – Moderate, 3 – Substantial, BT – Bloom's Taxonomy

18VLT12 DEVICE MODELING

(Common to VLSI Design & Applied Electronics branches)

L	T	P	Credit
3	0	0	3

Preamble	To model and analyze the performance of solid state devices using mathematical concepts
Prerequisites	Solid State Devices

UNIT – I **9**

Semiconductor Physics and Modeling of Passive Devices: Quantum Mechanical Concepts - Carrier Concentration - Transport Equation - Mobility and Resistivity - Carrier diffusion - Carrier Generation and Recombination - Continuity equation - Tunneling and High field effects - Modeling of resistors - Modeling of Capacitors - Modeling of Inductors.

UNIT – II **9**

Diode and Bipolar Device Modeling: Abrupt and linear graded PN junction - Ideal diode current equation - Static, Small signal and Large signal models of PN junction Diode - SPICE model for a Diode - Temperature and Area effects on Diode Model Parameters Transistor Action - Terminal currents – Switching - Static, Small signal and Large signal Eber-Moll models of BJT - Temperature and area effects.

UNIT – III **9**

MOSFET Modeling and Parameter Measurements: MOS Transistor - NMOS - PMOS - MOS Device equations - Threshold Voltage - Second order effects - Temperature Short Channel and Narrow Width Effect - Models for MOSFET.

UNIT – IV **9**

Noise Models and BSIM4 MOSFET Model: Noise Sources in MOSFET - Flicker Noise Modeling - Thermal Noise Modeling - BSIM4 MOSFET Model - Gate Dielectric Model - Enhanced Models for Effective DC and AC Channel Length and width - Threshold Voltage Model-I-V Model.

UNIT – V **9**

Other MOSFET Models: EKV Model - Model Features - Long Channel Drain Current Model - Modeling Second order Effects of Drain Current - Effect of Charge Sharing - Modeling of Charge storage Effects - Non-quasi static Modeling - Noise Models - Temperature Effects - MOS Model 9-MOSAI Model

Total: 45

REFERENCES:

1. Trond Ytterdal, Yuhua Cheng and Tor A. Fjeldly, "Device Modeling for Analog and RF CMOS Circuit Design", John Wiley & Sons Ltd., 2003.
2. Sze S.M., "Semiconductor Devices - Physics and Technology", 2nd Edition, John Wiley & Sons, New York, 2008.
3. Massobrio Giuseppe and Antognetti Paolo, "Semiconductor Device Modeling with SPICE", 2nd Edition, McGraw-Hill Inc., New York, 1998.
4. Tyagi M.S., "Intorduction to Semiconductor Materials and Devices", John Wiley, New York, 2003.
5. Ben G. Streetman, "Solid State Circuits", 5th Edition, Prentice Hall of India, New Delhi, 2005.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	realize the concepts of semiconductor physics	Understanding (K2)
CO2:	apply mathematical concepts to model basic semiconductor devices	Applying (K3)
CO3:	analyze the secondary effects of semiconductor physics using mathematical expressions	Analyzing (K4)
CO4:	analyze the effects of temperature and Area on the performance of semiconductor devices	Analyzing (K4)
CO5:	create models for MOSFETs	Creating (K6)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	2	2	2	
CO2			3	3	3	
CO3			2	3	2	
CO4			2	3	2	
CO5				1		

1 – Slight, 2 – Moderate, 3 – Substantial, BT – Bloom's Taxonomy

18VLT13 TESTING OF VLSI CIRCUITS

L	T	P	Credit
3	1	0	4

Preamble	To know the basics of VLSI test concepts, Test generation, DFT architectures, Built in Self Test and fault diagnosis.
Prerequisites	Digital Electronics

UNIT – I **9**

Basics of Testing and Fault Modelling: Introduction to Testing - Faults in digital circuits - Modeling of faults - Logical Fault Models - Fault detection - Fault location - Fault dominance - Logic Simulation - Types of simulation - Delay models - Gate level Event-driven simulation

UNIT – II **9**

Test Generation For Combinational And Sequential Circuits: Test generation for combinational logic circuits - Testable combinational logic circuit design - Test generation for sequential circuits - Design of testable sequential circuits.

UNIT – III **9**

Design For Testability: Design for Testability - Ad-hoc design - Generic scan based design - Classical scan based design - System level DFT approaches.

UNIT – IV **9**

Self-Test And Test Algorithms: Built-In Self Test - Test pattern generation for BIST - Circular BIST - BIST Architectures - Testable Memory Design - Test algorithms - Test generation for Embedded RAMs.

UNIT – V **9**

Fault Diagnosis: Logic Level Diagnosis - Diagnosis by UUT reduction - Fault Diagnosis for Combinational Circuits - Self-checking design - System Level Diagnosis.

Lecture:45, Tutorial:15, Total: 60

REFERENCES:

1. Abramovici M., Breuer M.A., and Friedman A.D., "Digital Systems and Testable Design", Jaico Publishing House, 2002.
2. Lala P.K., "Digital Circuit Testing and Testability", Academic Press, 2002.
3. Bushnell M.L. and Agrawal V.D., "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers, 2002.
4. Crouch A.L., "Design Test for Digital IC's and Embedded Core Systems", Prentice Hall International, 2002.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	distinguish between different fault models and types of simulation	Understanding (K2)
CO2:	analyze the various test generation methods for combinational and sequential circuits	Analyzing (K4)
CO3:	identify the design for testability techniques for combinational and sequential circuits	Applying (K3)
CO4:	compare the various Built In Self Test architectures	Analyzing (K4)
CO5:	review the various fault diagnosis approach for VLSI Systems	Understanding (K2)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	2	2	2	3
CO2			2	3	2	
CO3			3	3	3	
CO4			2	3	2	
CO5	3	3	2	2	2	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT – Bloom's Taxonomy

18VLC11 VLSI DESIGN TECHNIQUES

L	T	P	Credit
3	0	2	4

Preamble	To design the various combinational circuits and sequential circuits using VLSI Design Techniques
Prerequisites	Digital Electronics

UNIT – I **9**

Overview of VLSI Design Methodologies: VLSI Design Flow - Design Hierarchy - VLSI Design Styles - Review of Fabrication process - CMOS n-well process and SOI process - Layout Design Rules - Review of MOS Transistor Theory: Structure, Operation - MOSFET Current - Voltage Characteristics - Threshold Voltage - MOSFET Capacitances.

UNIT – II **9**

MOS Inverters Characteristics: Static: Resistive - Load Inverter - Inverters with MOSFET Load - CMOS Inverter. Switching: Delay Time definitions - Calculation of delay times - Inverter Design with Delay constraints - Power Delay product and Energy delay product.

UNIT – III **9**

Logic Design: CMOS Static and Complementary logic - CMOS Transmission Gates - Pass Transistor Circuit - Synchronous Dynamic Circuit - Dynamic CMOS Circuit Techniques - High performance CMOS Circuits.

UNIT – IV **9**

Sequential MOS Logic Circuits: Behavior of Bistable Elements - Latch Circuit - Flipflop Circuits - CMOS D Latch and Edge triggered Flipflop - Sense Amplifier based Flipflops.

UNIT – V **9**

VLSI Building Block Design: Arithmetic Building Block - Adders, Multipliers, Shifters, On chip Clock generation and Distribution - Memory Design.

List of Exercises / Experiments :

1. Layout Design for basic logic gates
2. Design and Analysis of CMOS Inverter
3. Sequential circuit design-I
4. Sequential circuit design-II
5. Design of Adders
6. Design of Multipliers
7. Design of Shifters
8. Design of Memory Design
9. Logic design using pass transistor and transmission gates
10. Multiplexer

Lecture:45, Practical:30, Total: 75

REFERENCES/ MANUALS/ SOFTWARES:	
1.	Sung-Mokang, Yusuf Leblebici and Chulwoo Kim, "CMOS Digital Integrated Circuits Analysis and Design", 4th Edition McGraw Hill, 2016.
2.	Jan M. Rabaey, "Digital Integrated Circuits", Prentice Hall, 2004.
3.	Neil H.E. Weste and Kamran Eshraghian, "Principles of CMOS VLSI Design", 3rd Edition, Pearson Education, ASIA, 2007.
4.	Pucknell, "Basic VLSI Design", Prentice Hall of India Publication, 1995.
5.	Micorwind tool
6.	Synopsys-Custom Designer tool

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	infer the steps in different fabrication methodologies	Understanding (K2)
CO2:	apply design rules and generate layout	Applying (K3)
CO3:	infer the characteristics of MoS transistor	Understanding (K2)
CO4:	analyze CMOS inverter with delay constraints	Analyzing (K4)
CO5:	design Combinational circuits in different logic styles	Manipulation(S2), Applying (K3)
CO6:	design Sequential circuits in different logic styles	Manipulation(S2), Applying (K3)
CO7:	design and analyze Adders and Multipliers	Manipulation(S2), Analyzing(K4)
CO8:	design and analyze Shifters and Memory	Manipulation(S2), Analyzing (K4)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	2	2	2	3
CO2			3	3	3	
CO3	3	3	2	2	2	3
CO4			2	3	2	
CO5			3	3	3	
CO6			3	3	3	
CO7			2	3	2	
CO8			2	3	2	

1 – Slight, 2 – Moderate, 3 – Substantial, BT – Bloom's Taxonomy

18VLC12 HDL FOR IC DESIGN

L	T	P	Credit
3	0	2	4

Preamble	To design and implement digital logic circuits using verilog in FPGA and to verify the functionality using Blue Spec
Prerequisites	Digital Electronics

UNIT – I **9**

Introduction to Verilog: Overview of digital design using Verilog HDL - Hierarchical Modeling Concepts - Basic Concepts - Gate level Modeling - Dataflow Modeling - Behaviour Modeling - Tasks and Functions - Switch level modeling.

UNIT – II **9**

Design using Verilog: Logic Synthesis using verilog HDL: Verilog HDL Synthesis - Synthesis Design Flow - Verification of the gate level net list - Modeling for logic synthesis - Example of sequential circuit synthesis.

UNIT – III **9**

Introduction to Bluespec System Verilog: Building the design - Multiple modules in a single package - Multiple package in single design - Data types – Variables – Assignments - Combinational circuits.

UNIT – IV **9**

Modeling using Bluespec System Verilog: Modelling Rules, registers, and FIFOs - Module hierarchy and interfaces – Scheduling - RWires and Wire types – Polymorphism - Advanced types and pattern.

UNIT – V **9**

System Design Using Bluespec System Verilog: Matching - Static elaboration - For-loops/while-loops – Expressions – Vectors - Finite State Machines (FSMs) - Importing existing RTL into a BSV design.

List of Exercises / Experiments :

1. Modeling of Sequential Digital Systems with Test benches
2. State Machine Design
3. Memory Design
4. Design and implementation of ALU, MAC using FPGA
5. Design and implementation of different adders using FPGA
6. Design and implementation of pipelined array multiplier using FPGA
7. Modeling Combinational circuits using Bluespec System verilog
8. FIFO design using Bluespec system verilog
9. Design on FSM using Bluespec system verilog

Lecture:45, Practical:30, Total: 75

REFERENCES:

1. Samir Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", Pearson Education New Delhi, 2003.
2. Chris Spear, "System Verilog for Verification: A Guide to Learning the Test bench Language Features", 2nd Edition, Springer, 2012.
3. https://ocw.mit.edu – Massachusetts Institute of Technology Open Courseware

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	apply digital design concepts and write verilog programs	Applying (K3)
CO2:	synthesis the digital circuit and implement in FPGA	Applying (K3)
CO3:	summarize the properties of blue spec system verilog	Understanding (K2)
CO4:	apply Bluespec system verilog for system design	Applying (K3)
CO5:	develop FSM based sequential systems using Bluespec system verilog	Applying (K3)
CO6:	design combinational and sequential system using verilog HDL	Applying (K3), Manipulation (S2)
CO7:	implement digital design in FPGA	Analyzing (K4), Imitation (S1)
CO8:	modelling digital circuit design using Bluespec system verilog	Analyzing (K4), Imitation (S1)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1			3	3	3	
CO2			3	3	3	
CO3	3	3	2	2	2	3
CO4			3	3	3	
CO5			3	3	3	
CO6			3	3	3	
CO7			2	3	2	
CO8			2	3	2	

1 – Slight, 2 – Moderate, 3 – Substantial, BT – Bloom's Taxonomy

18VLC21 ANALOG INTEGRATED CIRCUIT DESIGN				
	L	**T**	**P**	**Credit**
	3	**0**	**2**	**4**
Preamble	To focus on the concepts of MOSFETs and design of differential amplifiers, feedback amplifiers and their stability with practical knowledge.			
Prerequisites	Basic Electronics, Op-Amps fundamentals, Circuits and Networks			
UNIT – I				**9**
Basic MOS Device Physics and Single Stage Amplifiers: Basic MOS Device Physics – General Considerations, MOS I/V Characteristics, Second Order effects, MOS Device models- Short Channel Effects and Device Models. Single Stage Amplifiers – Basic Concepts, Common Source Stage, Source Follower, Common Gate Stage, Cascode Stage.				
UNIT – II				**9**
Differential Amplifiers and Current Mirrors: Differential Amplifiers – Single Ended and Differential Operation, Basic Differential Pair, Common-Mode Response, Differential Pair with MOS loads, Gilbert Cell. Passive and Active Current Mirrors – Basic Current Mirrors, Cascode Current Mirrors, Active Current Mirrors.				
UNIT – III				**9**
Frequency Response of Amplifiers and Noise: Frequency Response of Amplifiers – General Considerations, Common Source Stage, Source Followers, Common Gate Stage, Cascode Stage, Differential Pair. Noise – Types of Noise, Representation of Noise in circuits, Noise in single stage amplifiers, Noise in Differential Pairs.				
UNIT – IV				**9**
Feedback and Operational Amplifiers: Feedback Amplifiers- General Considerations, Feedback Topologies, Effect of Loading. Operational Amplifiers – General Considerations, One Stage Op Amps, Two Stage Op Amps, Gain Boosting, Common– Mode Feedback, Input Range limitations, Slew Rate, Power Supply Rejection, Noise in Op Amps.				
UNIT – V	**Stability and Frequency Compensation**			**9**
General Considerations-Multipole Systems- Phase Margin-Frequency Compensation-Compensating of Two-Stage Op Amps-Other Compensation Techniques.				
List of Exercises / Experiments :				
1. Understanding the Datasheet of Op-Amps. Introduction to op-amps and discussion on its characteristics by simulation and experiment				
2. Complete the design of two differential amplifiers, one of which uses emitter resistor (R_E) biasing, and one of which uses current mirror biasing.				
3. For the same circuit designed in experiment 2, Predict, measure and record AC voltage gain, common mode rejection ratio, and input and output impedance characteristics of a differential amplifier.				
4. For the same circuit designed in experiment 2, Predict, measure and record DC voltages and currents in differential amplifiers which employ two basic types of constant current biasing.				
5. For the same circuit designed in experiment 2, Observe the impact on common mode voltage gain, Acm, and common mode rejection ratio, CMRR, as a current mirror is substituted for the emitter resistor (R_E) of a simple differential amplifier.				
6. Determine the frequency response of typical operational amplifiers in both open loop and closed loop opamp configurations using PSPICE.				
7. Simulation of Op-Amp based applications.				

8. Analysis of frequency response of current series and current shunt feedback topologies.

9. Analysis of frequency response of voltage series and voltage shunt feedback topologies.

Lecture:45, Practical:30, Total: 75

REFERENCES / MANUALS / SOFTWARES:

1. Razavi B., "Design of Analog CMOS Integrated Circuits", McGraw Hill Edition, 2002.
2. Paul R. Gray, Robert G. Meyer, "Analysis and Design of Analog Integrated Circuits", 4th Edition, Wiley, 2001.
3. Johns D. A. and Martin K., "Analog Integrated Circuit Design", Wiley, 1997.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	comprehend the concepts of MOS devices physics	Understanding (K2)
CO2:	infer the single stage amplifiers, differential amplifiers and current mirrors	Understanding (K2)
CO3:	analyze single stage amplifiers, differential amplifier	Analyzing (K4)
CO4:	analyze the different current mirrors	Analyzing (K4)
CO5:	appreciate the frequency compensation techniques	Understanding (K2)
CO6:	examine the frequency response of amplifiers and the effects of noise in amplifiers	Analyzing (K4), Imitation (S1)
CO7:	design feedback amplifiers	Analyzing (K4), Manipulation (S2)
CO8:	design operational amplifier based analog circuits	Analyzing (K4), Manipulation (S2)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	2	2	2	3
CO2	3	3	2	2	2	3
CO3			2	3	2	
CO4			2	3	2	
CO5			2	3	2	
CO6			2	3	2	
CO7	3	3	2	2	2	3
CO8			2	3	2	

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

18VLC22 APPLICATION SPECIFIC INTEGRATED CIRCUITS

L	T	P	Credit
3	0	2	4

Preamble	To know the different programmable ASICs, logic cells, I/O cells and interconnect and to learn how synthesis and physical design flow in carried out in an ASIC design.
Prerequisites	VLSI Design Techniques

UNIT – I **9**

Introduction to ASICs, CMOS Logic and ASIC Library Design: Types of ASICs - Design flow - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort.

UNIT – II **9**

Programmable ASICs, Programmable ASIC Logic Cells And Programmable ASIC I/O Cells: Anti fuse - static RAM - EPROM and EEPROM technology - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

UNIT – III **9**

Programmable ASIC Interconnect: Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX9000 - Altera FLEX.

UNIT – IV **9**

Design and Synthesis: Design systems - Half gate ASIC –Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation-.Logic synthesis – Logic Simulation - Design and synthesis of various circuits.

UNIT – V **9**

Physical Design: ASIC Partitioning - floor planning- placement and routing – power and clocking strategies - DRC.

List of Exercises / Experiments:

1. Design, simulation and synthesis of logic gates
2. Design, simulation and synthesis of Adders
3. Design, simulation and synthesis of multipliers
4. Design, simulation and synthesis of memory
5. Design, simulation and synthesis of Finite state machine
6. Floor Planning, Routing and Placement procedures
7. Analysis of Circuits - Power Planning, Layout generation, LVS and Back annotation, Total power estimation

Lecture:45, Practical:30, Total: 75

REFERENCES / MANUALS / SOFTWARES:

1. Smith M.J.S., "Application - Specific Integrated Circuits", 10th Reprint, Pearson, 2001.
2. Steve Kilts, "Advanced FPGA Design", 1st Edition, Wiley Inter-Science, 2007.
3. Roger Woods, John McAllister, Dr. Ying Yi, Gaye Lightbod, "FPGA-based Implementation of Signal Processing Systems", Wiley, 2008.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	demonstrate ASIC design flow and comprehend the types of ASIC	Understanding (K2)
CO2:	realize the issues involved in ASIC design, including design, role of transistor, logical effort and programming technology	Understanding (K2)
CO3:	analyze the issues involved in logic cells, I/O cells and interconnect	Applying (K3)
CO4:	perform simulation and synthesis of the design using different programmable ASIC design software	Applying (K3)
CO5:	analyze the algorithms used in partitioning, Floorplanning, placement, routing, power and clock design for ASIC	Applying (K3)
CO6:	perform the partitioning ,floorplanning and Placement for the ASIC	Applying (K3), Manipulation (S2)
CO7:	perform power and clock routing in ASIC	Applying (K3), Manipulation (S2)
CO8:	analyze performance metrics of the design	Analyzing (K4), Manipulation (S2)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	2	2	2	3
CO2	3	3	2	2	2	3
CO3			3	3	3	
CO4			3	3	3	
CO5			3	3	3	
CO6			3	3	3	
CO7			3	3	3	
CO8			2	3	2	

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

18VLT21 VLSI SIGNAL PROCESSING

(Common to VLSI Design and Applied Electronics branches)

L	T	P	Credit
3	0	0	3

Preamble	To apply the concepts of VLSI techniques to real time signal processing
Prerequisites	Digital Signal Processing

UNIT – I **9**

Introduction to DSP Systems: Introduction To DSP Systems -Typical DSP algorithms. **Iteration Bound** – data flow graph representations, loop bound and iteration bound, Algorithms For Computing Iteration Bound, Iteration Bound of Multirate Data Flow Graphs. **Pipelining and Parallel Processing:** Pipelining of FIR digital filters, parallel processing, pipelining and parallel processing for low power.

UNIT – II **9**

Retiming: Definitions and properties retiming techniques; solving systems of inequalities, retiming techniques. **Unfolding:** Algorithm for unfolding, properties of unfolding, critical path unfolding and retiming applications of unfolding- sample period reduction and parallel processing application.

UNIT – III **9**

Systolic Architecture Design: Design methodology, FIR systolic arrays. **Bit Level Arithmetic Architectures:** Parallel Multipliers, Bit-Serial Multipliers, Bit-Serial Filter Design and Implementation, Canonic Signed Digit Arithmetic, Distributed Arithmetic.

UNIT – IV **9**

Fast Convolution: Fast convolution – Cook-Toom algorithm, modified Cook-Took algorithm – Wino grad Algorithm, Modified Wino grad Algorithm. **Algorithmic Strength Reduction:** Algorithmic strength reduction in Filters-Parallel FIR Filters, DCT and Inverse DCT. **Pipelined and Parallel Recursive filters Adaptive Filters:** Pipelining in first- order IIR filters, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.

UNIT – V **9**

Scaling, Round off Noise: Scaling and Round off Noise- State variable Description of digital filters, Scaling and round off noise computation, Round off noise in pipelined I order IIR filters. **Lattice Structure:** Introduction, Schur algorithm, Digital basic Lattice Filters, Derivation of One-Multiplier Lattice Filter, Derivation of Normalized Lattice filter. **Numerical Strength Reduction:** Introduction, Sub expression Elimination, Multiple Constant Multiplication, Sub expression Sharing in Digital Filters, Additive and Multiplicative Number Splitting.

Total: 45

REFERENCES:

1. Parhi K. Keshab, "VLSI Digital Signal Processing Systems, Design and Implementation", Reprint, John Wiley, Inter Science, New York, 2008.
2. Isamail, Mohammed and Fiez, Terri, "Analog VLSI Signal and Information Processing", McGraw-Hill, New York, 2007.
3. www.pdf-search-engine.com/vlsi-signal-processing-pdf.html

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	compute the iteration bound of a circuit	Applying (K3)
CO2:	perform pipelining and parallel processing in FIR systems to achieve high speed and low power	Applying (K3)
CO3:	improve the speed of digital system through transformation techniques	Applying (K3)
CO4:	apply systolic and bit level architectures to improve the efficiency of VLSI circuits	Applying (K3)
CO5:	use of proper techniques for parallel processing design for scaling and roundoff noise computation	Applying (K3)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1			3	3	3	
CO2			3	3	3	
CO3			3	3	3	
CO4			3	3	3	
CO5			3	3	3	

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

18COE04 ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY

(Common to Communication Systems,VLSI Design, Applied Electronics & Power Electronics and Drives branches)

L	T	P	Credit
3	0	0	3

Preamble	To expose the basics and fundamentals of Electromagnetic Interference and Compatibility in Communication System Design and to know the concepts of EMI Coupling Principles, EMI Measurements and Control techniques and the methodologies of EMI based PCB design.
Prerequisites	Electromagnetic Principles

UNIT – I **9**

EMI Environment: EMI/EMC concepts and definitions, Sources of EMI, conducted and radiated EMI, Transient EMI, Time domain Vs Frequency domain EMI, Units of measurement parameters, Emission and immunity concepts, ESD.

UNIT – II **9**

EMI Coupling Principles: Conducted, Radiated and Transient Coupling, Common Impedance Ground Coupling, Radiated Common Mode and Ground Loop Coupling, Radiated Differential Mode Coupling, Near Field Cable to Cable Coupling, Power Mains and Power Supply coupling.

UNIT – III **9**

EMI/EMC Standards and Measurements: Civilian standards - FCC, CISPR,I EC, EN, Military standards - MIL STD 461D/462, EMI Test Instruments /Systems, EMI Shielded Chamber, Open Area Test Site, TEM Cell, Sensors/Injectors/Couplers, Test beds for ESD and EFT, Military Test Method and Procedures (462).

UNIT – IV **9**

EMI Control Techniques: EMI Control Techniques : Shielding, Filtering, Grounding, Bonding, Isolation Transformer, Transient Suppressors, Cable Routing, Signal Control, Component Selection and Mounting

UNIT – V **9**

EMC Design of PCBs: PCB Traces Cross Talk, Impedance Control, Power Distribution Decoupling, Zoning, Motherboard Designs and Propagation Delay Performance Models.

Total: 45

REFERENCES:

1. Ott W. Henry, "Noise Reduction Techniques in Electronic Systems", 2nd Edition, John Wiley & Sons, New York, 2008.
2. Kodali V.P., "Engineering EMC Principles, Measurements and Technologies", 2nd Edition, IEEE Press, London, 2006.
3. Keiser Bernhard, "Principles of Electromagnetic Compatibility", 3rd Edition, Artech House, Dedham, 1987.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	estimate the EMI and analyze in time domain and frequency domain	Analyzing (K4)
CO2:	compare the various EMI coupling methods	Evaluating (K5)
CO3:	conduct the EMI measurement for civilian and military appliances	Analyzing (K4)
CO4:	device the EMI control techniques	Applying (K3)
CO5:	evaluate the PCB'S and motherboards EMI performance and design the EMC circuits	Creating (K6)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	2	2		1	
CO2	1	2	3			
CO3	2	3	2	2	3	
CO4	2		3	2		
CO5			2	1	3	2

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

18COE09 DSP PROCESSOR ARCHITECTURE AND PROGRAMMING

(Common to Communication Systems,VLSI Design & Embedded Systems branches)

L	T	P	Credit
2	0	2	3

Preamble	To design the parameters of filters and implement it in real time DSP hardware.
Prerequisites	Digital Signal Processing

UNIT – I **6**

Fundamentals of Programmable DSPs: Multiplier and Multiplier accumulator (MAC) – Modified Bus Structures and Memory access in Programmable DSPs – Multiple access memory – Multi-port memory – VLIW architecture- Pipelining – Special Addressing modes in P-DSPs – On chip Peripherals

UNIT – II **6**

TMS320C54XX: Fundamentals of Programmable DSPs - Architecture of TMS320C54X-54X Buses-Memory organization-Computational Units-Pipeline operation-On-chip peripherals – Address Generation Units- Addressing modes and instruction set- assembly language instructions -Introduction to Code Composer studio

UNIT – III **6**

TMS320C6X: Architecture of TMS320C6X – Computational units-Addressing modes – Memory architecture- pipeline operation- instruction set- assembly language instructions

UNIT – IV **6**

Blackfin Processor(BF537): Architecture of BF537- Computational units - Internal Memory organization- System interrupts – Direct Memory Access- on-chip peripherals-ALU-MAC-DAG Units-Addressing modes-Assembly language instructions- Timers –Interrupts-Serial ports-UART-Simple programs

UNIT – V **6**

Applications Using TMS320C54X/C6X/BF537: Program development - Software Development Tools- The Assembler and the Assembly Source File Filter design- Linker and Memory Allocation -DSP Software Development Steps- Speech Digitization-Encoding and Decoding-Image compression-Restoration-Adaptive Echo cancellation-Modulation

List of Experiments:

1. Basic Signal operations using 54x.
2. Convolution using c54x and c6713x
3. FIR and IIR filter using C6713
4. Basic operations and convolution using BF 537
5. Speech and Audio application development using BF537

Lecture:30, Practical:30, Total: 60

REFERENCES / MANUALS / SOFTWARES:

1. Sen M. Kuo, Woon–Seng S. Gan, "Digital Signal Processors: Architecture, Implementation and Applications", 1st Edition, Prentice Hall, 2009.
2. Woon-Seng Gan, Sen M. Kuo, "Embedded Signal Processing with the Microsignal Architecture", John

	Wiley & Sons Inc. Publications, 2007.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	infer the basic concepts of DSP processor	Understanding (K2)
CO2:	apply programming concepts to develop simple and real time applications programs using c54x processor	Applying (K3)
CO3:	apply programming concepts to develop simple and real time applications using c6x processor	Applying (K3)
CO4:	apply programming concepts to develop simple and real time applications using BF 537 processor	Applying (K3)
CO5:	analyze the performance of DSP processors like TMS320C54X/C6X/BF537	Analyzing (K4)
CO6:	demonstrate the concepts of DSP using DSP processor	Applying (K3), Manipulation (S2)
CO7:	design digital filters using DSP processors	Applying (K3), Manipulation (S2)
CO8:	demonstrate speech/audio applications using DSP processor	Applying (K3), Manipulation (S2)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3				2	
CO2	3				3	
CO3	3				3	
CO4	3				3	
CO5	3	3			3	
CO6	3				3	
CO7	3				3	
CO8	3				3	

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

18VLE01 COMPUTER AIDED DESIGN OF VLSI CIRCUITS				
	L	**T**	**P**	**Credit**
	2	**1**	**0**	**3**
Preamble	To give an overview of the VLSI physical design and understand CAD algorithms used in VLSI physical design automation field.			
Prerequisites	ASIC Design			
UNIT – I				**6**
Design Methodologies: Introduction to VLSI Design methodologies – Review of VLSI Design automation tools –Algorithmic Graph Theory and Computational Complexity – Tractable and Intractable problems – general purpose methods for combinatorial optimization problems				
UNIT – II				**6**
Partitioning, Placement and Floorplanning: Placement and Partitioning – Circuit representation – Placement algorithms – Partitioning - Partitioning algorithms - Floorplanning concepts – shape functions and floorplan sizing – Floorplanning based on Simulated Annealing				
UNIT – III				**6**
Routing and Compaction: Routing – Types of local routing problems – Area routing – channel routing – global routing –algorithms for global routing. Compaction- Layout Compaction –Design rules –problem formulation –algorithms for constraint graph compaction.				
UNIT – IV				**6**
Logic Simulation: Simulation – Gate-level modeling and simulation –Switch-level modeling and simulation. Introduction to Combinational Logic Synthesis –Binary Decision Diagrams – ROBDD - ROBDD principles, implementation, construction and manipulation.				
UNIT – V				**6**
High Level Synthesis: Hardware models –Internal representation –Allocation assignment and scheduling – Simple scheduling algorithm –Assignment problem –High level transformations.				
Lecture:30, Tutorial:15, Total: 45				
REFERENCES:				
1.	Gerez S.H., "Algorithms for VLSI Design Automation", Reprint, John Wiley & Sons, New York, 2000.			
2.	Sherwani N.A., "Algorithms for VLSI Physical Design Automation", 3rd Edition, Kluwar Academic Publishers, Boston, 2002.			
3.	Sarafzadeh C.K. Wong, "An Introduction to VLSI Physical Design", Reprint, McGraw Hill International Edition, 2007.			

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	comprehend the concepts and properties associated with graph theory	Understanding (K2)
CO2:	demonstrate the concepts of physical design process such as partitioning, floor planning, placement and routing	Understanding (K2)
CO3:	apply the concepts of design optimization algorithms and their application to VLSI physical design automation	Applying (K3)
CO4:	realize the concepts of simulation and synthesis in VLSI design automation	Understanding (K2)
CO5:	analyze CAD design problems using algorithmic methods for VLSI physical design automation	Analyzing (K4)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	2	2	2	3
CO2	3	3	2	2	2	3
CO3			3	3	3	
CO4		3	2	2	2	3
CO5	3		2	3	2	

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

18VLE02 DESIGN OF SEMICONDUCTOR MEMORIES

(Common to VLSI Design and Embedded Systems branches)

L	T	P	Credit
3	0	0	3

Preamble	To study the architectures for SRAM and DRAM, various non-volatile memories, fault modeling and testing of memories for fault detection and the radiation hardening process and issues for memory.
Prerequisites	Solid State Devices

UNIT – I **9**

Random Access Memory Technologies: SRAM Cell Structures-MOS SRAM Architecture-MOS SRAM Cell and Peripheral Circuit Operation- Bipolar SRAM Technologies-Silicon On Insulator (SOl) Technology-Advanced SRAM Architectures and Technologies-Application Specific SRAMs DRAM Technology Development- CMOS DRAMs- DRAMs Cell Theory and Advanced Cell Structures- BiCMOS, DRAMs-Soft Error Failures in DRAMs- Advanced DRAM Designs and Architecture- Application Specific DRAMs.

UNIT – II **9**

Nonvolatile Memories : Masked Read-Only Memories (ROMs)- High Density ROMs- Programmable Read-Only Memories (PROMs)- Bipolar PROMs- CMOS PROMs- Erasable(UV) Programmable Road-Only Memories (EPROMs)- Floating-Gate PROM Cell- One-Time Programmable (OTP) EPROMS- Electrically Erasable PROMs (EEPROMs)- EEPROM Technology and Architecture- Nonvolatile SRAM- Flash Memories (EPROMs or EEPROM)- Advanced Flash Memory Architecture.

UNIT – III **9**

Memory Fault Modeling And Testing: RAM Fault Modeling, Electrical Testing, Peusdo Random Testing-Megabit DRAM Testing- Nonvolatile Memory Modeling and Testing- IDDQ Fault Modeling and Testing-Application Specific Memory Testing.

UNIT – IV **9**

Semiconductor Memory Reliability: General Reliability Issues- RAM Failure Modes and Mechanism-Nonvolatile Memory Reliability- Reliability Modeling and Failure Rate Prediction- Design for Reliability-Reliability Test Structures- Reliability Screening and Qualification.

UNIT – V **9**

Packaging Technologies: Radiation Effects- Single Event Phenomenon (SEP)- Radiation Hardening Techniques- Radiation Hardening Process and Design Issues- Radiation Hardened Memory Characteristics-Radiation Hardness Assurance and Testing - Radiation Dosimetry-Water Level Radiation Testing and Test Structures. Ferroelectric Random Access Memories (FRAMs)- Gallium Arsenide (GaAs) FRAMs- Analog Memories- Magnetoresistive Random Access Memories (MRAMs)- Experimental Memory Devices. Memory Hybrids and MCMs (2D)-Memory Stacks and MCMs (3D)-Memory MCM Testing and Reliability Issues-Memory Cards- High Density Memory Packaging Future Directions.

Total: 45

REFERENCES:

1. Sharma K. Ashok, “Semiconductor Memories: Technology, Testing, and Reliability”, Wiley-IEEE Press, New York, 2002.
2. Sharma K. Ashok, “Advanced Semiconductor Memories, Architectures, Designs and Applications”, Wiley-IEEE Press, New York, 2009.
3. Krzysztof Hiewski, Santosh K. Kurinec, “Nanoscale Semiconductor Memories”, CRC Press, 2017.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	comprehend the micro level operations of random access memories	Understanding (K2)
CO2:	analyze the need of non-volatile memories and their applications	Analyzing (K4)
CO3:	design the fault free memory systems by fault modeling techniques	Evaluating (K5)
CO4:	analyze and design the memory architectures by considering the radiation effects	Analyzing (K4)
CO5:	identify the packages for memories	Understanding (K2)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	2	2	2	3
CO2			2	3	2	
CO3			1	2	1	
CO4			2	3	2	
CO5	3	3	2	2	2	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

18VLE03 LOW POWER VLSI DESIGN

(Common to VLSI Design and Applied Electronics branches)

L	T	P	Credit
3	1	0	4

Preamble	To design the combinational and sequential circuits with minimum power consumption and to anlayse the various power optimization methods and techniques to reduce power consumption.
Prerequisites	VLSI Design Techniques

UNIT – I **9**

Power dissipation in CMOS: Hierarchy of limits of power – Sources of power consumption – Physics of power dissipation in CMOS FET devices – Basic principle of low power design

UNIT – II **9**

Power Optimization: Logic level power optimization – Circuit level low power design – circuit techniques for reducing power consumption in adders and multipliers.

UNIT – III **9**

Design of Low Power CMOS Circuits: Computer arithmetic techniques for low power system – reducing power consumption in memories – low power clock, Inter connect and layout design – Advanced techniques –Special techniques.

UNIT – IV **9**

Power Estimation: Power Estimation techniques – logic power estimation – Simulation power analysis – Probabilistic power analysis.

UNIT – V **9**

Software Design for Low Power: Sources of Software Power dissipation - Power Estimation - Power Optimization - Automated low power code generation - Codesign for low power.

Lecture:45, Tutorial:15, Total: 60

REFERENCES:

1. Kaushik Roy and Prasad S.C., "Low Power CMOS VLSI Circuit Design", Reprint, Wiley, 2014.
2. Dimitrios Soudris, Chirstian Pignet, Costas Goutis, "Designing CMOS Circuits for Low Power", 4th Edition, Kluwer, Springer, 2010.
3. Kulo J.B. and Lou J.H., "Low Voltage CMOS VLSI Circuits", Wiley, 1999.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	enumerate the different sources of power dissipation in CMOS	Understanding (K2)
CO2:	analyze various power optimization technique at circuit level	Analyzing (K4)
CO3:	design of low power circuits at architecture level	Creating (K6)
CO4:	use of simulation and probabilistic method of power analysis	Analyzing (K4)
CO5:	perform power estimation and optimization at programming level	Evaluating (K5)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	2	1		1	2
CO2			2	3	2	
CO3				1		3
CO4				3	2	
CO5			1	2	1	

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

18VLE04 RECONFIGURABLE ARCHITECTURES FOR VLSI				
	L	**T**	**P**	**Credit**
	3	**0**	**0**	**3**

Preamble	To comprehend and apply different reconfigurable architectures in FPGA
Prerequisites	VLSI Design techniques, VLSI Signal Processing

UNIT – I **9**

Device Architecture: General Purpose Computing vs Reconfigurable Computing – Simple Programmable Logic Devices – Complex Programmable Logic Devices – FPGAs – Device Architecture - Case Studies.

UNIT – II **9**

Reconfigurable Computing Architectures and Systems: Reconfigurable Processing Fabric Architectures – RPF Integration into Traditional Computing Systems – Reconfigurable Computing Systems – Case Studies – Reconfiguration Management.

UNIT – III **9**

Programming Reconfigurable Systems: Compute Models - Programming FPGA Applications in HDL - Compiling C for Spatial Computing – Operating System Support for Reconfigurable Computing.

UNIT – IV **9**

Mapping Designs to Reconfigurable Platforms: The Design Flow - Technology Mapping - FPGA Placement - Datapath composition - Retiming, Repipelining, and C-slow Retiming – Configuration Bit stream Generation.

UNIT – V **9**

Application Development with FPGAs: Implementing Applications with FPGAs - Case Studies of FPGA Applications - Signal Processing - Image Processing - Compression - Bioinformatics Application.

Total: 45

REFERENCES:

1.	Scott Hauck and Andre Dehon (Eds.), "Reconfigurable Computing – The Theory and Practice of FPGA-Based Computation", 1st Edition, Elsevier / Morgan Kaufmann, 2007.
2.	Maya B. Gokhale and Paul S. Graham, "Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays", Springer, 2005.
3.	Christophe Bobda, "Introduction to Reconfigurable Computing – Architectures, Algorithms and Applications", 1st Edition, Springer, 2007.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	comprehend the different computing and models	Understanding (K2)
CO2:	discuss the different reconfigurable computing architecture and systems	Analyzing (K4)
CO3:	programming reconfigurable systems	Evaluating (K5)
CO4:	mapping the design into different platforms	Evaluating (K5)
CO5:	analyze and develop reconfigurable applications	Creating (K6)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	2	2	2	3
CO2			2	3	2	
CO3			1	2	1	
CO4			1	2	1	
CO5				1		

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

18VLE05 MIXED SIGNAL VLSI DESIGN					
		L	**T**	**P**	**Credit**
		3	**0**	**0**	**3**
Preamble	To build the advanced CMOS VLSI Design with practical aspect of mixed signal VLSI blocks such as data converters using HDL				
Prerequisites	CMOS Analog IC design, VLSI design				
UNIT – I					**9**
Introduction to Active Filters and Switched Capacitor Filters: Switched capacitor filters: Switched capacitor resistors - amplifiers – comparators - sample and hold circuits – Integrator- Biquad					
UNIT – II					**9**
Continuous Time Filters: Introduction to Gm - C filters - bipolar transconductors - CMOS Transconductors using Triode transistors, active transistors - BiCMOS transconductors – MOSFET C Filters - Tuning Circuitry - Dynamic range performance -Elementary transconductor building block- First and Second order filters					
UNIT – III					**9**
Digital To Analog and Analog To Digital Converters: Non-idealities in the DAC - Types of DAC's: Current switched, Resistive, Charge redistribution (capacitive), Hybrid, segmented DAC's - Techniques for improving linearity - Analog to Digital Converters: quantization errors - non-idealities - types of ADC's: Flash, two step, pipelined, successive approximation, folding ADC's.					
UNIT – IV					**9**
Sigma Delta Converters: Over sampled converters - over sampling without noise & with noise - implementation imperfections - first order modulator - decimation filters - second order modulator - sigma delta DAC & ADC's					
UNIT – V					**9**
Analog And Mixed Signal Extensions To HDL: Introduction - Language design objectives - Theory of differential algebraic equations - the 1076 .1 Language - Tolerance groups - Conservative systems - Time and the simulation cycle - A/D and D/A Interaction - Quiescent Point - Frequency domain modeling and examples-analog extensions to Verilog: Introduction - data types –Expressions – Signals-Analog behavior –Hierarchical Structures –Mixed signal Interaction					
					Total: 45

REFERENCES:

1. David A. Johns and Ken Martin, "Analog Integrated Circuit Design", 2nd Edition, John Wiley & Sons, 2008.
2. Rudy van de Plassche, "CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters", 2nd Edition, Kluwer, 2007.
3. Antoniou, "Digital Filters Analysis and Design and Signal Processing Applications", 2nd Edition, Tata McGraw Hill, 2007.
4. Phillip Allen and Douglas Holberg "CMOS Analog Circuit Design", Oxford University Press, 2012.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	comprehend the concepts of active filters and switched capacitor filters	Understanding (K2)
CO2:	comprehend the concepts of continuous time filters and its performance	Understanding (K2)
CO3:	analyze digital to analog & analog to digital converters	Analyzing (K4)
CO4:	examine sigma delta converters	Evaluating (K5)
CO5:	design analog and mixed signal circuits using HDL	Creating (K6)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	2	2	2	3
CO2	3	3	2	2	2	3
CO3			2	3	2	
CO4			1	2	1	
CO5				1		

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

18VLE06 SUPERVISED MACHINE LEARNING ALGORITHMS

(Common to VLSI Design & Embedded Systems branches)

L	T	P	Credit
3	0	0	3

Preamble	To focus on supervised machine learning algorithms to create simple, interpretable models to solve classification and regression problem.
Prerequisites	Linear Algebra, calculus

UNIT – I **9**

Discriminative Algorithms: Cost function –LMS Algorithm – The normal Equations-Probability interpretation-locally weighted linear regression-logistic regression-generalized linear models-Application to prediction.

UNIT – II **9**

Generative Algorithms: Generative Models: Gaussian Discriminant Analysis(GDA)-Naïve Bayes- Laplace smoothing-Marginal classifier: Support Vector Machine (SVM) as optimal Margin classifier-Application to Classification.

UNIT – III **9**

Neural Networks: ANN Architecture- Parameter Initialization -Forward Propagation- Activation Functions (Sigmoid,tanh,relu)-Training and Optimization with back propagation-Learning Boolean Functions.

UNIT – IV **9**

Convolutional Neural Networks (CNN) : Convolution kernel-Pooling (Max Pooling, fractional Pooling)-Strides-Fully Connected Layers –Loss functions – MiniBatch Training -Optimization – Application to MNIST image classification.

UNIT – V **9**

Hyper Parameter Tuning: Regularization: Bias-Variance-Bias-variance Trade off- Initialization of parameters (Xavier)-Cross Validation-Data Augmentation-dropouts-Batch Normalization.

Total: 45

REFERENCES:

1. Christopher M. Bishop, "Pattern Recognition and Machine Learning", Springer-Verlag New York, Reprint, 2010.
2. Trevor Hastie, "The Elements of Statistical Learning: Data Mining, Inference, and Prediction", 2nd Edition, Springer, 2009.
3. UCI Machine Learning repository: http://archive.ics.uci.edu/ml/index.php

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	analyse and apply discriminative algorithms for classification and regression problems	Analyzing (K4)
CO2:	validate a generative model based algorithm for classification and regression problems	Analyzing (K4)
CO3:	analyse the designed ANN for a real time application using BPN	Analyzing (K4)
CO4:	develop a CNN model for image analysis	Applying (K3)
CO5:	analyse various error metrics used in supervised learning	Analyzing (K4)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1			2	3	2	
CO2			2	3	2	
CO3			2	3	2	
CO4			3	3	3	
CO5			2	3	2	

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

18VLE07 VLSI FOR BIOMEDICAL APPLICATIONS

L	T	P	Credit
3	0	0	3

Preamble	To comprehend and apply the various low power techniques for Biomedical circuits.
Prerequisites	Low Power VLSI Design and RF VLSI Design

UNIT – I **9**

Low-Power Analog and Biomedical Circuits: Low power transimpedance amplifiers and photoreceptors- Low power transconductance amplifiers and scaling laws for power in analog circuits- Low-power filters and resonators- Low power current- mode circuits - Ultra-low-power and neuron-inspired analog-to-digital conversion for biomedical system.

UNIT – II **9**

Low-Power RF and Energy-Harvesting Circuits for Biomedical Systems: Wireless inductive power links for medical implants - Energy-harvesting RF antenna power links - Low-power RF telemetry in biomedical implants.

UNIT – III **9**

Biomedical Electronic Systems: Ultra-low-power implantable medical electronics- cochlear implants or bionic ears-an ultra low power programmable analog bionic ear processor-low power electrode stimulation-highly miniature electrode –stimulation –Brain machine interfaces for the blind-Brain machine interface for paralysis, speech, and other disorders. Ultra-low-power noninvasive medical electronics -Analog integrated-circuit switched-capacitor model of the heart – the electrocardiogram- A micro power electrocardiogram amplifier -Low-power pulse oximetry - Battery-free tags for body sensor networks -Intra-body galvanic communication networks - Biomolecular sensing.

UNIT – IV **9**

Principles for Ultra-Low-Power Analog and Digital Design: Digital design- Sizing and topologies for robust sub threshold operation-Types of power dissipation-energy efficiency-Optimization of energy efficiency-Varying the power-supply voltage and threshold voltage-gated clocks-Basics of adiabatic computing-adiabatic clocks- Architectures and algorithms for improving energy efficiency. Analog and mixed-signal design -Power consumption in analog and digital systems-low power hand- The optimum point for digitization in mixed-signal system Common themes in low-power analog and digital design-The Shannon limit for energy efficiency-Collective analog or hybrid computation-HSMs: general-purpose mixed-signal systems with feedback-General principles for low-power mixed-signal system design-The evolution of low-power design-Actuators and sensors.

UNIT – V **9**

Bio-Inspired Systems: Neuromorphic electronics- Transmission-line theory- The cochlea: biology, motivations, theory, and RF-cochlea design- A bio-inspired analog vocal tract- Bio-inspired vision architectures Hybrid analog-digital computation in the brain- Spike-based hybrid computers- Energy efficiency in neurobiological systems Cytomorphic electronics: cell-inspired electronics for systems and synthetic biology- Electronic analogies of chemical reactions- Log-domain current-mode models of chemical reactions and protein-protein networks- Analog circuit models of gene-protein dynamics- Logic-like operations in gene-protein circuits- Circuits-and-feedback techniques for systems and synthetic biology- Hybrid analog-digital computation in cells and neurons.

Total: 45

REFERENCES:

1. Rahul Sarpeshkar, "Ultra Low Power Bioelectronics: Fundamentals, Biomedical Applications, and Bio-Inspired Systems" 1st Edition, Cambridge University Press, 2011.
2. Kris Iniewski, "VLSI Circuit Design for Biomedical Applications", 1st Edition, Artech House Publishers, 2008.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	acquire the concepts of low power amplifier circuits	Understanding (K2)
CO2:	comprehend RF CMOS circuits for Biomedical applications	Understanding (K2)
CO3:	correlate the analogy of biological components with low power circuits	Applying (K3)
CO4:	design analog and mixed signal biomedical circuits	Analyzing (K4)
CO5:	interpret various bioinspired systems	Understanding (K2)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	2	2	2	3
CO2	3	3	2	2	2	3
CO3			3	3	3	
CO4			2	3	2	
CO5	3	3	2	2	2	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT - Bloom's Taxonomy

18VLE08 VLSI TECHNOLOGY				
	L	**T**	**P**	**Credit**
	3	**0**	**0**	**3**
Preamble	To infer the foundations in MOS and CMOS fabrication process.			
Prerequisites	Semiconductor Theory			

UNIT – I	**9**
Crystal Growth, Wafer Preparation, Epitaxy and Oxidation: Electronic Grade Silicon, Czochralski crystal growing, Silicon Shaping, processing consideration, Vapor phase Epitaxy, Molecular Beam Epitaxy, Silicon on Insulators, Growth Mechanism and kinetics, Thin Oxides, Oxidation Techniques and Systems, Oxide properties, Redistribution of Dopants at interface, Oxidation of Poly Silicon, Oxidation induced Defects.	

UNIT – II	**9**
Lithography and Relative Plasma Etching: Optical Lithography, Electron Lithography, X-Ray Lithography, Ion Lithography, Plasma properties, Feature Size control and Anisotropic Etch mechanism, relative Plasma Etching techniques and Equipments	

UNIT – III	**9**
Deposition and Diffusion: Deposition process, Polysilicon, Silicon Dioxide- Silicon Nitride- plasma assisted Deposition, Models of Diffusion in Solids, Flick's one dimensional Diffusion Equation – Atomic Diffusion Mechanism –Measurement techniques	

UNIT – IV	**9**
Ion implementation and Metallization: Range theory- Implant equipment. Annealing-Shallow junction – High energy implantation – Metallization Applications- Metallization choices- Physical vapor deposition – Patterning	

UNIT – V	**9**
VLSI Process Integration and Packaging of VLSI Devices: NMOS IC Technology – CMOS IC Technology – MOS Memory IC technology – Bipolar IC Technology – IC Fabrication. Package types– banking design consideration – VLSI assembly technology – Package fabrication technology	

Total: 45

REFERENCES:

1. Sze S.M., "VLSI Technology", 2nd Edition, McGraw-Hill, New York, 2017.
2. Mukherjee Amar, "Introduction to NMOS and CMOS VLSI System Design", Prentice Hall India, New Delhi, Digitized 2007.
3. Plummer D. James, Deal D. Michael and Griffin B. Peter, "Silicon VLSI Technology: Fundamentals Practice and Modeling", Prentice Hall India, New Delhi, 2009.
4. Chen Wai Kai, "VLSI Technology", CRC Press, London, 2003.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	summarize the approach for wafer preparation, Epitaxy and Oxidation	Understanding (K2)
CO2:	distinguish the various methods for lithography and plasma etching	Understanding (K2)
CO3:	illustrate the various Deposition and diffusion process	Understanding (K2)
CO4:	infer the process of ion implantation and metallization	Understanding (K2)
CO5:	realize the various IC technology and Package types	Understanding (K2)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	2	2	2	3
CO2	3	3	2	2	2	3
CO3	3	3	2	2	2	3
CO4	3	3	2	2	2	3
CO5	3	3	2	2	2	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT – Bloom's Taxonomy

18MME13 MEMS DESIGN

(Common to Mechatronics, CADCAM, Engineering Design, VLSI Design, Applied Electronics, Power Electronics and Drives & Control and Instrumentation Engineering branches)

L	T	P	Credit
3	0	0	3

Preamble: This course equips the students to understand the concepts of Micro mechatronics and apply the knowledge of micro fabrication techniques for various applications.

Prerequisites: Sensors and Instrumentation and Bridge course mechanical

UNIT – I **9**

Materials for MEMS and Scaling Laws: Overview - Microsystems and microelectronics - Working principle of Microsystems - Si as a substrate material - Mechanical properties - Silicon compounds - Silicon piezo resistors - Gallium arsenide - Quartz-piezoelectric crystals - Polymer - Scaling laws in Miniaturization.

UNIT – II **9**

Micro Sensors, Micro Actuators: Micro sensors - Micro actuation techniques - Micro actuators – Micromotors – Microvalves – Micro grippers – Micro accelerometer: introduction, types, actuating principles, design rules, modeling and simulation, verification and testing, applications.

UNIT – III **9**

Mechanics for Microsystem Design: Static bending of thin plates - Mechanical vibration - Thermo mechanics - Thermal stresses - Fracture mechanics - Stress intensity factors, fracture toughness and interfacial fracture mechanics-Thin film Mechanics-Overview of Finite Element Stress Analysis.

UNIT – IV **9**

Fabrication Process and Micromachining: Photolithography - Ion implantation - Diffusion – Oxidation – CVD - Physical vapor deposition - Deposition by epitaxy - Etching process- Bulk Micro manufacturing - Surface micro machining – LIGA –SLIGA.

UNIT – V **9**

Micro System Design, Packaging and Applications: Design considerations - Process design - Mechanical design – Mechanical Design using Finite Element Method-Micro system packaging – Die level - Device level - System level – Packaging techniques - Die preparation - Surface bonding - Wire bonding – Sealing - Applications of micro system in Automotive industry: Bio medical, Aerospace and Telecommunications – CAD tools to design a MEMS device.

Total: 45

REFERENCES:

1. Tai-Ran Hsu, "MEMS and Microsystems Design and Manufacture", Tata McGraw-Hill, New Delhi, 2008.
2. Mohamed Gad-el-Hak, "The MEMS Handbook", CRC Press, 2009.
3. Bao M.H., "Micromechanical Transducers: Pressure sensors, accelrometers, and gyroscopes", Elsevier, New York, 2000.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	interpret the concepts of MEMS materials and scaling laws	Remembering (K1)
CO2:	explain the principles of micro sensors and actuators	Understanding (K2)
CO3:	apply the mechanics for micro system design	Applying (K3)
CO4:	design and fabrication of microsystem	Applying (K3)
CO5:	design of microsystem packaging and application	Applying (K3)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		3	2		2
CO2	3		3	3		2
CO3	2		2			
CO4	3		3	3		2
CO5	3		3	3		2

1 – Slight, 2 – Moderate, 3 – Substantial, BT – Bloom's Taxonomy

18MIE14 QUANTUM INFORMATION AND COMPUTING

L	T	P	Credit
3	0	0	3

Preamble	To provide a broad overview of the main ideas of the field of quantum computation. It also describes the fundamental elements of quantum circuits, different quantum algorithms, quantum noise with error correction.
Prerequisites	Applied physics, Mathematics

UNIT – I **9**

Introduction to Quantum Computation: Linear algebra - Quantum mechanics - Superdense coding - Density operator - EPR and the Bell inequality.

UNIT – II **9**

Quantum Circuits: Single qubit operations - Controlled operations - Measurement - Universal quantum gates - Simulation of quantum systems.

UNIT – III **9**

Quantum Algorithms: The quantum Fourier transform - General applications of the quantum Fourier Transform - Quantum search algorithms.

UNIT – IV **9**

Noise and Error Correction: Quantum noise and quantum operations - Quantum error-correction - Fault-tolerant quantum computation.

UNIT – V **9**

Quantum Information Theory: Data compression - Entanglement as a physical resource - Quantum cryptography.

Total: 45

REFERENCES:

1. Nielsen M. A. andChuang I. L., "Quantum Computation and Quantum Information", 10th Anniversary Edition, Cambridge University Press, 2010.
2. Scott Aaronson, "Quantum Computing Since Democritus", 1st Edition, Cambridge University Press, 2013.
3. Phillip Kaye, Raymond Laflamme, Michele Mosca, "An Introduction to Quantum Computing", 1st Edition, Oxford University Press, Reprint, 2010.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	describe the quantum mechanics using linear algebra	Understanding (K2)
CO2:	familiar with qubits and designing of quantum gates	Analyzing (K4)
CO3:	realize the quantum parallelism by using simplest quantum algorithms	Applying (K3)
CO4:	understand real-world quantum information processing	Understanding (K2)
CO5:	analyze the information carrying properties of quantum states	Understanding (K2)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2		2			
CO2	3		3		3	
CO3	3		3			2
CO4	3		2			2
CO5	3		2			2

1 – Slight, 2 – Moderate, 3 – Substantial, BT – Bloom's Taxonomy

18VLE09 HARDWARE SOFTWARE CO-DESIGN				
	L	**T**	**P**	**Credit**
	3	**0**	**0**	**3**
Preamble	To develop an integrated application development environment of hardware/software codesign of embedded system			
Prerequisites	RTOS			
UNIT – I				**9**
Design Consideration: Platform-Based Design – System Modeling – Video Coding – Image Processing – Cryptography - Digital Communication**.**				
UNIT – II				**9**
System Level Design: Abstraction Levels – Algorithm Level Verification – Transaction Level Modeling – System Level Development Tools.				
UNIT – III				**9**
Embedded Processor Design: Specific Instruction-Set - Data Level Parallelism – Instruction Level Parallelism – Thread Level Parallelism				
UNIT – IV				**9**
Parallel Compiler: Vectorization - Simdization – ILP Scheduling – Threading - Compiler Technique – Compiler Infrastructures				
UNIT – V				**9**
Real-Time Operating System for PLX: PRRP Scheduler - Memory Management – Communication and Synchronization Primitives - Multimedia Applications in RTOS for PLX – Application Development Environment.				
				Total: 45

REFERENCES:

1. Sao-jie Chen , Guang - Huei Lin, Pao -Ann Hsiung and Yu-Hen Hu, “Hardware Software Co-Design of a Multimedia SOC Platform”, Springer, 2009.
2. Jorgen Staunstrup, Wayne Wolf, “Hardware/Software Co-Design: Principles and Practice”, Kluwer Academic Pub, 1997.
3. Patrick Schaumont, “A Practical Introduction to Hardware/Software Co design”, 3rd Edition, Springer, 2014.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	acquire knowledge about system level modeling and image and video encoding	Understanding (K2)
CO2:	perform algorithm level verification and learn system development tools	Applying (K3)
CO3:	distinguish between different levels of parallelism	Understanding (K2)
CO4:	infer scheduling and compiler techniques	Understanding (K2)
CO5:	interpret the requirements of Real time Operating Systems and develop an integrated application development environment of hardware/software codesign of embedded system	Creating (K6)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	2	2	2	3
CO2			3	3	3	
CO3	3	3	2	2	2	3
CO4	3	3	2	2	2	3
CO5				1		

1 – Slight, 2 – Moderate, 3 – Substantial, BT – Bloom's Taxonomy

18VLE10 INTELLECTUAL PROPERTY BASED VLSI DESIGN				
	L	**T**	**P**	**Credit**
	3	**0**	**0**	**3**
Preamble	To provide an overview of the security problems in modern VLSI design for the protection of VLSI design IPs from FPGA design to standard-cell placement, from high-level synthesis solutions to gate-level netlist place-and-route, and from advanced CAD tools to physical design algorithms.			
Prerequisites	VLSI Design			
UNIT – I				**9**
VLSI and its Fabrication: IC manufacturing, CMOS technology, IP based design,Fabrication process-Transistors, Wires and Via, Fabrication Theory reliability				
UNIT – II				**9**
Combinational Logic Networks: Combinational Logic Functions, Static Complementary Gates, Switch Logic, Alternate Gate circuits, Low power gates, Gates as IP, Combinational network delay, Logic and Interconnect design, Power Optimization, Switch logic network				
UNIT – III				**9**
Sequential Machine: Latch and Flip flop, System design and Clocking, Performance analysis, power optimization, Design validation and testing				
UNIT – IV				**9**
Subsystem Design: Combinational Shifter, Arithmetic Circuits, High Density memory, Image Sensors, FPGA,PLA, Buses and NoC, Data paths, Subsystems as IP.				
UNIT – V				**9**
Architecture Design: HDL, Register-Transfer Design, Pipelining, High Level Synthesis, Architecture for Low power, GALS systems, Architecture Testing, IP Components, Design Methodologies, Multiprocessor System-on-chip Design.				
				Total: 45
REFERENCES:				
1.	Wayne Wolf, "Modern VLSI Design: IP-based Design", 4th Edition, Pearson Education, 2009.			
2.	Qu gang and Miodrag Potkonjak, "Intellectual Property Protection in VLSI Designs: Theory and Practice", 1st Edition, Kluwer Academic Publishers, 2003.			

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	comprehend the manufacturing process and basic properties of transistors	Understanding (K2)
CO2:	design of combinational logic gates and networks using various logic styles	Applying (K3)
CO3:	design and validation of sequential systems	Applying (K3)
CO4:	design of subsystems for various application	Analyzing (K4)
CO5:	development of architecture for various application	Evaluating (K5)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	2	2	2	3
CO2			3	3	3	
CO3			3	3	3	
CO4			2	3	2	
CO5			1	2	1	

1 – Slight, 2 – Moderate, 3 – Substantial, BT – Bloom's Taxonomy

18VLE11 NANOELECTRONICS

L	T	P	Credit
3	0	0	3

Preamble	To provide a foundation for the nano device fabrication and to apply in the field of sensors technology.
Prerequisites	Digital Electronics

UNIT – I **9**

Materials for Nanoelectronics: Semiconductors, Crystal lattices: bonding in crystals, Electron energy bands, Semiconductor heterostructures , Lattice-matched and pseudomorphic heterostructures ,Inorganic nanowires, Organic semiconductors , Carbon nanomaterials: nanotubes and fullerenes.

UNIT – II **9**

Nanoelectronics and Nanocomputer Architectures: Introduction to Nanocomputers, Nanocomputer Architecture, Quantum DOT cellular Automata (QCA), QCA circuits, Single electron circuits, molecular circuits, Logic switches – Interface engineering – Properties (Self-organization, Size-dependent) – Limitations.

UNIT – III **9**

Spintronics: Introduction, Overview, History & Background, Generation of Spin Polarization Theories of spin Injection, spin relaxation and spin dephasing, Spintronic devices and applications, spin filters, spin diodes, spin transistors.

UNIT – IV **9**

Transport in Nanostrcutures: Time and length scales of the electrons in solids, Statistics of the electrons in solids and nanostructures, Fermi statistics for electrons, the density of states of electrons in nanostructures, Electron transport in nanostructures. Electrons in quantum wells: Single modulation-doped heterojunctions, Numerical analysis of a single heterojunction, Control of charge transfer, Electrons in quantum wires, Electron transport in quantum wires, Electrons in quantum dots.

UNIT – V **9**

Memory Devices And Sensors: Memory devices and sensors – Nano ferroelectrics – Ferroelectric random access memory – Fe-RAM circuit design –ferroelectric thin film properties and integration – calorimetric - sensors electrochemical cells – surface and bulk acoustic devices – gas sensitive FETs – resistive semiconductor gas sensors –electronic noses – identification of hazardous solvents and gases – semiconductor sensor array

Total: 45

REFERENCES:

1. Karl Goser and Jan Dienstuhl, "Nanoelectronics and Nanosystems: From Transistor to Molecular and Quantum Devices", Springer, 2014.
2. Rainer Waser, "Nano Electronics and Information Technology: Advanced Electronic Materials and Novel Devices", 3rd Edition, Wiley, 2012.
3. Sadamichi Maekawa, "Concepts in Spintronics", Oxford Science Publications, 2006.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	describe the energy bands of semiconducting materials and nanostructures (Nanowire, Nanotube, Fullerene)	Understanding (K2)
CO2:	explain the architecture of nanocomputer and logic for quantum cellular automata	Understanding (K2)
CO3:	apply the concept of spin polarization in spintronic devices (Filters, Diodes, Transistors)	Applying (K3)
CO4:	distinguish the electron transport in different nanostructures	Understanding (K2)
CO5:	describe the concept of FeRAM, supercapacitor and gas sensor	Understanding (K3)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	2	2	2	3
CO2	3	3	2	2	2	3
CO3			3	3	3	
CO4	3	3	2	2	2	3
CO5	3	3	2	2	2	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT – Bloom's Taxonomy

18VLE12 NATURE INSPIRED OPTIMIZATION TECHNIQUES

(Common to VLSI Design , Communication Systems, Embedded Systems, Computer Science and Engineering & Mechatronics branches)

L	T	P	Credit
3	0	0	3

Preamble	To acquaint and familiarize with different types of optimization techniques, solving optimization problems, implementing computational techniques, abstracting mathematical results and proofs etc.
Prerequisites	Linear algebra and Calculus

UNIT – I **9**

Introduction to Algorithms: Newton's Method – Optimization - Search for Optimality - No-Free-Lunch Theorems - Nature-Inspired Metaheuristics - Brief History of Metaheuristics. **Analysis of Algorithms:** Introduction - Analysis of Optimization Algorithms - Nature-Inspired Algorithms - Parameter Tuning and Parameter Control.

UNIT – II **9**

Simulated Annealing: Annealing and Boltzmann Distribution - Parameters - SA Algorithm - Unconstrained Optimization - Basic Convergence Properties - SA Behavior in Practice - Stochastic Tunneling. **Genetic Algorithms** : Introduction - Genetic Algorithms - Role of Genetic Operators - Choice of Parameters - GA Variants - Schema Theorem - Convergence Analysis

UNIT – III **9**

Particle Swarm Optimization: Swarm Intelligence - PSO Algorithm - Accelerated PSO – Implementation - Convergence Analysis - Binary PSO – Problems. **Cat Swarm Optimization:** Natural Process of the Cat Swarm - Optimization Algorithm – Flowchart - Performance of the CSO Algorithm.

UNIT – IV **9**

TLBO Algorithm: Introduction - Mapping a Classroom into the Teaching-Learning-Based optimization – Flowchart- Problems. **Cuckoo Search:** Cuckoo Life Style - Details of COA – flowchart - Cuckoos' Initial Residence Locations - Cuckoos' Egg Laying Approach - Cuckoos Immigration - Capabilities of COA. **Bat Algorithms:** Echolocation of Bats - Bat Algorithms – Implementation - Binary Bat Algorithms - Variants of the Bat Algorithm - Convergence Analysis.

UNIT – V **9**

Other Algorithms: Ant Algorithms - Bee-Inspired Algorithms - Harmony Search - Hybrid Algorithms.

Total: 45

REFERENCES:

1. Xin-She Yang, "Nature-Inspired Optimization Algorithms", 1st Edition, Elsevier, 2014.
2. Omid Bozorg-Haddad, "Advanced Optimization by Nature-Inspired Algorithms" Springer Volume 720, 2018.
3. Srikanta Patnaik, Xin-She Yang, Kazumi Nakamatsu, "Nature-Inspired Computing and Optimization Theory and Applications", Springer Series, 2017.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	infer the basic concepts of optimization techniques	Understanding (K2)
CO2:	identify the parameter which is to be optimized for an application	Analyzing (K4)
CO3:	analyze and develop mathematical model of different optimization algorithms	Analyzing (K4)
CO4:	select suitable optimization algorithm for a real time application	Applying (K3)
CO5:	recommend solutions, analyses, and limitations of models	Analyzing (K4)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	2	2	2	3
CO2			2	3	2	
CO3			2	3	2	
CO4			3	3	3	
CO5			2	3	2	

1 – Slight, 2 – Moderate, 3 – Substantial, BT – Bloom's Taxonomy

18VLE13 NETWORK ON CHIP				
	L	**T**	**P**	**Credit**
	3	**0**	**0**	**3**
Preamble	To understand the different network architectures and concepts of NOC.			
Prerequisites	Computer Communication Networks			

UNIT – I	**9**
Uses of Interconnection Networks: Processor-Memory Interconnect - I/O Interconnect - Packet Switching Fabric - Network Basics - Topology - Routing - Flow Control - Router Architecture - Performance of Interconnection - Case study with a simple interconnection network..	

UNIT – II	**9**
Topology Basics: Channels and Nodes - Direct and Indirect Networks - Cuts and Bisections - Paths - Symmetry - Traffic Patterns - Performance - Throughput and Maximum Channel Load - Latency - Path Diversity - Case Study: Butterfly and Torus Networks.	

UNIT – III	**9**
Non-Blocking Networks: Non-Blocking vs. Non-Interfering Networks - Crossbar Networks - Close Networks - Beneˇs Networks - Sorting Networks. **Slicing and Dicing:** Concentrators and Distributors - Bit Slicing - Dimension Slicing - Channel Slicing - Slicing Multistage Networks.	

UNIT – IV	**9**
Routing Basics: A Routing Example - Taxonomy of Routing Algorithms - The Routing Relation - Deterministic Routing - Oblivious Routing - Adaptive Routing - Routing Mechanics**.**	

UNIT – V	**9**
Flow Control Basics: Resources and Allocation Units - Buffer less Flow Control - Circuit Switching - Buffered Flow Control. **Deadlock and Livelock:** Deadlock - Deadlock Avoidance - Adaptive Routing - Deadlock Recovery. Quality of Service.	

Total: 45

REFERENCES:

1. William James Dally and Brian Towles, "Principles and Practices of Interconnection Networks", 1st Edition, Morgan Kaufmann Publishers, 2004.
2. Santanu Kundu and Santanu Chattopadhyay, "Network-on-Chip: The Next Generation of System on-Chip Integration", CRC Press, 2014.
3. Giovanni De Micheli and Luca Benini, "Networks on Chips: Technology and Tools", 1st Edition, Academic Press, 2006.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	summarize the interconnection networks	Understanding (K2)
CO2:	comprehend the basics of network topology	Understanding (K2)
CO3:	classify the different types of networks	Understanding (K2)
CO4:	illustrate routing algorithms	Applying (K3)
CO5:	explain the basics of flow control, deadlock and livelock	Understanding (K2)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	2	2	2	3
CO2	3	3	2	2	2	3
CO3	3	3	2	2	2	3
CO4			3	3	3	
CO5	3	3	2	2	2	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT – Bloom's Taxonomy

18VLE14 GENETIC ALGORITHMS FOR VLSI CIRCUITS				
	L	**T**	**P**	**Credit**
	3	**0**	**0**	**3**

Preamble	To perform VLSI design optimization, layout generation and chip testing using genetic algorithm for developing efficient computer aided design tools.
Prerequisites	ASIC Design

UNIT – I	**9**
Introduction: GA Technology-Steady State Algorithm-Fitness Scaling-Inversion	
UNIT – II	**9**
Physical Design of VLSI: GA for VLSI Design, Layout and Test automation-partitioning- automatic placement, routing technology, Mapping for FPGA -Automatic test generation-Partitioning algorithm Taxonomy - Multiway Partitioning.	
UNIT – III	**9**
Standard Cell and Macro Cell Placement: Hybrid genetic – genetic encoding-local improvement-WDFR-Comparison of GA with other methods-Standard cell placement-GASP algorithm-Macro Cell Placement-unified algorithm.	
UNIT – IV	**9**
Macrocell Routing and FPGA Technology Mapping: Global routing-FPGA technology mapping-circuit generation-test generation in a GA frame work-test generation procedures.	
UNIT – V	**9**
Power Estimation: Application of GA to Peak power estimation - Standard cell placement-GA for ATG-problem encoding- fitness function-GA vs Conventional algorithm.	
	Total: 45

REFERENCES:

1. Pinaki Mazumder, Rudnick E.M., "Genetic Algorithm for VLSI Design, Layout and Test Automation", 1st Impression, Prentice Hall, 2014.
2. Ricardo Sal Zebulum, Macro Aurelio Pacheco, Marley Maria B.R. Vellasco, Marley Maria Bernard Vellasco, "Evolution Electronics: Automatic Design of Electronic Circuits and Systems Genetic Algorithms", 1st Edition, CRC Press, December 2001.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	comprehend the concepts of genetic algorithm	Understanding (K2)
CO2:	realize the concepts of physical design process such as partitioning, floorplanning, placement and routing	Remembering (K1)
CO3:	calculate power estimation in VLSI Layout using genetic algorithm	Applying (K3)
CO4:	apply genetic algorithm for automatic test pattern generation in VLSI circuits	Applying (K3)
CO5:	analyze CAD design problems using genetic algorithm for VLSI physical design automation	Analyzing (K4)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	2	2	2	3
CO2	2	2	1		1	2
CO3			3	3	3	
CO4			3	3	3	
CO5			2	3	2	

1 – Slight, 2 – Moderate, 3 – Substantial, BT – Bloom's Taxonomy

18VLE15 RF VLSI DESIGN

L	T	P	Credit
3	0	0	3

Preamble	To infer the concepts of CMOS RF circuits and to design RF devices, circuits, and systems at microwave regime.
Prerequisites	Analog IC Design

UNIT – I **9**

CMOS Physics, Transceiver Specifications and Architectures: Introduction to MOSFET Physics, Noise: Thermal, shot, flicker, popcorn noise, Two port Noise theory, Noise Figure, THD, IP2, IP3, Sensitivity, SFDR, Phase noise - Specification distribution over a communication link, Homodyne Receiver, Heterodyne Receiver, Image reject, Low IF Receiver Architectures Direct up conversion Transmitter, Two step up conversion Transmitter

UNIT – II **9**

Impedance Matching and Amplifiers: S-parameters with Smith chart, Passive IC components, Impedance matching networks, Common Gate, Common Source Amplifiers, OC Time constants in bandwidth estimation and enhancement, High frequency amplifier design, Power match and Noise match, Single ended and Differential LNAs, Terminated with Resistors and Source Degeneration LNAs.

UNIT – III **9**

Feedback Systems and Power Amplifiers: Stability of feedback systems: Gain and phase margin, Root-locus techniques, Time and Frequency domain considerations, Compensation, General model – Class A, AB, B, C, D, E and F amplifiers, Power amplifier Linearization Techniques, Efficiency boosting techniques, ACPR metric, Design considerations

UNIT – IV **9**

Mixers and Oscillators: Mixer characteristics, Non-linear based mixers, Quadratic mixers, Multiplier based mixers, Single balanced and double balanced mixers, subsampling mixers, Oscillators describing Functions, Colpitts oscillators Resonators, Tuned Oscillators, Negative resistance oscillators, Phase noise.

UNIT – V **9**

PLL and Frequency Synthesizers: Linearised Model, Noise properties, Phase detectors, Loop filters and Charge pumps, Integer-N frequency synthesizers, Direct Digital Frequency synthesizers

Total: 45

REFERENCES:

1. Lee T., "Design of CMOS RF Integrated Circuits", 2nd Edition, Cambridge, 2004.
2. Razavi B., "RF Microelectronics", 2nd Edition, Pearson Education, Reprint 2012.
3. Jan Crols and Michiel Steyaert, "CMOS Wireless Transceiver Design", Kluwer Academic Publishers, 1997.
4. Razavi B., "Design of Analog CMOS Integrated Circuits", 2nd Edition, McGraw Hill, 2001.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	differentiate the noises associated with CMOS technology and to comprehend the RF receive operation	Understanding (K2)
CO2:	interpret the concept of impedance matching	Understanding (K2)
CO3:	analyze the parameters of RF amplifier design	Analyzing (K4)
CO4:	design RF mixers and oscillators for IC implementations	Applying (K3)
CO5:	comprehend PLL and synthesizer architectures and their performance	Understanding (K2)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	2	2	2	3
CO2	3	3	2	2	2	3
CO3			2	3	2	
CO4			3	3	3	
CO5	3	3	2	2	2	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT – Bloom's Taxonomy

18VLE16 VLSI FOR WIRELESS COMMUNICATION				
	L	**T**	**P**	**Credit**
	3	**0**	**0**	**3**
Preamble	To identify the basic wireless communication techniques and describe the design of low-noise amplifier (LNAs), mixers, A/D converters, oscillators and also to analyzes phase noise in frequency synthesizers			
Prerequisites	VLSI Design Techniques, Communication theory			

UNIT – I	**9**

Wireless Communication Basics: Wireless Communication Standards- Digital communication systems- minimum bandwidth requirement, the Shanon limit. Overview of modulation schemes- classical channel- wireless channel description- Path loss- multipath fading.

UNIT – II	**9**

Transceiver Architecture: Noise Figure- Intermediation- Super heterodyne- Homodyne receiver- Software Radio- Transceiver design constraints- baseband subsystem design- RF subsystem design.

UNIT – III	**9**

Low Power Design Techniques: Source of power dissipation- estimation of power dissipation- reducing power dissipation at device and circuit levels- low voltage and low power operation- reducing power dissipation at architecture and algorithm levels.

UNIT – IV	**9**

Wireless Circuits: LSI Design of LNA-wideband and narrow band. Active mixer- balancing- qualitative description of the Gilbert mixer- Conversion Gain. Passive mixer- Switching mixer. Sampling mixer.

UNIT – V	**9**

Phase Locked Loops and Frequency Synthesizers: Operation of the PLL- Phase Detectors- Frequency Dividers - Oscillator Design. Frequency synthesizer parameters and Techniques- Analyzing phase noise in frequency synthesizers.

Total: 45

REFERENCES:

1. Emad N. Farag and Mohamed I. Elmasry, "Mixed Signal VLSI Wireless Design - Circuits and Systems", Kindle Edition, Kluwer Academic Publishers, 2000.
2. Bosco Leung, "VLSI for Wireless Communication", 2nd Edition, Springer, 2011.
3. Thomas H. Lee, "The Design of CMOS Radio – Frequency Integrated Circuits", 2nd Edition, Cambridge University Press, 2003.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	recall the basic concepts of wireless communication	Remembering (K1)
CO2:	summarize the transceiver architecture for wireless communication	Understanding (K2)
CO3:	apply the low power design techniques at different levels of system design	Applying (K3)
CO4:	distinguish the different types of design of mixers for wireless communication	Understanding (K2)
CO5:	infer oscillators for PLL and analyse phase noise in frequency synthesizers	Analyzing (K4)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	2	1		1	2
CO2	3	3	2	2	2	3
CO3			3	3	3	
CO4	3	3	2	2	2	3
CO5			2	3	2	

1 – Slight, 2 – Moderate, 3 – Substantial, BT – Bloom's Taxonomy