KONGU ENGINEERING COLLEGE

(Autonomous Institution Affiliated to Anna University, Chennai)

PERUNDURAI ERODE – 638 060

TAMILNADU INDIA

Estd : 1984

REGULATIONS, CURRICULUM & SYLLABI - 2020

(CHOICE BASED CREDIT SYSTEM AND OUTCOME BASED EDUCATION)

(For the students admitted during 2020 - 2021 and onwards)

MASTER OF ENGINEERING DEGREE IN EMBEDDED SYSTEMS

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

KONGU
Assuring the Best

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KONGU ENGINEERING COLLEGE
PERUNDURAI ERODE – 638 060
(Autonomous)

INSTITUTE VISION

To be a centre of excellence for development and dissemination of knowledge in Applied Sciences, Technology, Engineering and Management for the Nation and beyond.

INSTITUTE MISSION

We are committed to value based Education, Research and Consultancy in Engineering and Management and to bring out technically competent, ethically strong and quality professionals to keep our Nation ahead in the competitive knowledge intensive world.

QUALITY POLICY

We are committed to

- Provide value based quality education for the development of students as competent and responsible citizens.
- Contribute to the nation and beyond through research and development
- Continuously improve our services

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VISION

To be a centre of excellence for development and dissemination of knowledge in Electronics and Communication Engineering for the Nation and beyond

MISSION

Department of Electronics and Communication Engineering is committed to:

MS1: To impart industry and research based quality education for developing value based electronics and communication engineers

MS2: To enrich the academic activities by continual improvement in the teaching learning process

MS3: To infuse confidence in the minds of students to develop as entrepreneurs

MS4: To develop expertise for consultancy activities by providing thrust for Industry Institute Interaction

MS5: To endeavour for constant upgradation of technical expertise for producing competent professionals to cater to the needs of the society and to meet the global challenges

PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

Post Graduates of Electronics and Communication Engineering will

PEO1: Succeed in industry and research by applying knowledge of digital systems, embedded systems, signal and image processing and networking.

PEO2: Identify, design and analyze solutions to solve real world problems in embedded domain

PEO3: Demonstrate soft skills , professional and ethical values and aptitude for life long learning needed for a successful professional career

MAPPING OF MISSION STATEMENTS (MS) WITH PEOs

MS\PEO	PEO1	PEO2	PEO3
MS1	3	3	3
MS2	2	2	3
MS3	3	3	3
MS4	3	3	1
MS5	2	2	3

1 – Slight, 2 – Moderate, 3 – Substantial

PROGRAM OUTCOMES (POs)

M.E(Embedded System) Graduates will be able to:

PO1: Independently carry out research/investigation and development work to solve practical problems

PO2: Write and present a substantial technical report/document

PO3: Apply the knowledge of digital system, embedded systems, signal & image processing and networking to provide solutions for real time embedded applications

PO4: Use research based knowledge includes design, analyze and interpret data for Automotive Electronics, Consumer Electronics, Robotics, Automation and Process Control Industries to undertake multi disciplinary industrial projects and solve complex problems using modern tools.

PO5: Demonstrate self confidence and communication skills to become an efficient team leader

PO6: Continue to improve the professional value through lifelong learning and hold ethical responsibility for the professional and the society at large

MAPPING OF PEOs WITH POs

PEO\PO	PO1	PO2	PO3	PO4	PO5	PO6
PEO1	3	3	3	3	2	2
PEO2	3	2	3	3	2	2
PEO3	3	1	2	2	3	3

1 – Slight, 2 – Moderate, 3 – Substantial

KONGU ENGINEERING COLLEGE, PERUNDURAI, ERODE – 638060

(An Autonomous Institution Affiliated to Anna University)

REGULATIONS 2020

CHOICE BASED CREDIT SYSTEM AND OUTCOME BASED EDUCATION

MASTER OF ENGINEERING (ME) / MASTER OF TECHNOLOGY (MTech) DEGREE PROGRAMMES

These regulations are applicable to all candidates admitted into ME/MTech Degree programmes from the academic year 2020 – 2021 onwards.

1. DEFINITIONS AND NOMENCLATURE

In these Regulations, unless otherwise specified:

i. "University" means ANNA UNIVERSITY, Chennai.

ii. "College" means KONGU ENGINEERING COLLEGE.

iii. "Programme" means Master of Engineering (ME) / Master of Technology (MTech) Degree programme

iv. "Branch" means specialization or discipline of ME/MTech Degree programme, like Construction Engineering and Management, Information Technology, etc.

v. "Course" means a Theory / Theory cum Practical / Practical course that is normally studied in a semester like Engineering Design Methodology, Machine Learning Techniques, etc.

vi. "Credit" means a numerical value allocated to each course to describe the candidate's workload required per week.

vii. "Grade" means the letter grade assigned to each course based on the marks range specified.

viii. "Grade point" means a numerical value (0 to 10) allocated based on the grade assigned to each course.

ix. "Principal" means Chairman, Academic Council of the College.

x. "Controller of Examinations" means authorized person who is responsible for all examination related activities of the College.

xi. "Head of the Department" means Head of the Department concerned of the College.

2. PROGRAMMES AND BRANCHES OF STUDY

The following programmes and branches of study approved by Anna University, Chennai and All India Council for Technical Education, New Delhi are offered by the College.

Programme	Branch
ME	Construction Engineering and Management
	Structural Engineering
	Engineering Design
	Mechatronics Engineering
	VLSI Design
	Embedded Systems
	Power Electronics and Drives
	Control and Instrumentation Engineering
	Computer Science and Engineering
MTech	Information Technology
	Chemical Engineering
	Food Technology

3. ADMISSION REQUIREMENTS

Candidates seeking admission to the first semester of the ME/MTech Degree programme shall be required to have passed an appropriate qualifying Degree Examination of Anna University or any examination of any other University or authority accepted by the Anna University, Chennai as equivalent thereto, subject to amendments as may be made by the Anna University, Chennai from time to time. The candidates shall also be required to satisfy all other conditions of admission prescribed by the Anna University, Chennai and Directorate of Technical Education, Chennai from time to time.

4. STRUCTURE OF PROGRAMMES

4.1 Categorisation of Courses

The ME / MTech programme shall have a curriculum with syllabi comprising of theory, theory cum practical, practical courses in each semester and project work, internship,etc that have been approved by the respective Board of Studies and Academic Council of the College. All the programmes have well defined Programme Outcomes (PO) and Programme Educational Objectives (PEOs) as per Outcome Based Education (OBE). The content of each course is designed based on the Course Outcomes (CO). The courses shall be categorized as follows:

i. Foundation Courses (FC)

ii. Professional Core (PC) Courses

iii. Professional Elective (PE) Courses

iv. Open Elective (OE) Courses

v. Employability Enhancement Courses (EC) like Innovative Project, Internship cum Project work in Industry or elsewhere, Project Work

4.2 Credit Assignment

Each course is assigned certain number of credits as follows:

Contact period per week	Credits
1 Lecture / Tutorial Period	1
2 Practical Periods	1
2 Project Work Periods	1
40 Training /Internship Periods	1

The minimum number of credits to complete the ME/MTech programme is 72.

4.3 Employability Enhancement Courses

A candidate shall be offered with the employability enhancement courses like innovative project, internship cum project work and project work during the programme to gain/exhibit the knowledge/skills.

4.3.1 Innovative Project

A candidate shall earn two credits by successfully completing the project by using his/her innovations in second semester during his/her programme.

4.3.2 Internship cum Project Work

The curriculum enables a candidate to go for full time internship during the third semester and can earn credits through it for his/her academics vide clause 7.6 and clause 7.12. Such candidate shall earn the minimum number of credits as mentioned in the third semester of the curriculum other than internship by either fast track mode or through approved courses in online mode or by self study mode. Such candidate can earn the number of credits for the internship same as that of Project Work in the third semester. Assessment procedure is to be followed as specified in the guidelines approved by the Academic Council.

4.3.4 Project Work

A candidate shall earn nine credits by successfully completing the project work in fourth semester during the programme inside the campus or in industries.

4.4 Value Added Courses / Online Courses / Self Study Courses

The candidates may optionally undergo Value Added Courses / Online Courses / Self Study Courses as elective courses.

4.4.1 **Value Added Courses:** Value Added courses each with One / Two credits shall be offered by the college with the prior approval from respective Board of Studies. A candidate can earn a maximum of three credits through value added courses during the entire duration of the programme.

4.4.2 **Online Courses:** Candidates may be permitted to earn credits for online courses, offered by NPTEL / SWAYAM / a University / Other Agencies, approved by respective Board of Studies.

4.4.3 **Self Study Courses:** The Department may offer an elective course as a self study course. The syllabus of the course shall be approved by the respective Board of Studies. However, mode of assessment for a self study course will be the same as that used for other courses. The candidates shall study such courses on their own under the guidance of member of the faculty. Self study course is limited to one per semester.

4.4.4 The elective courses in the final year may be exempted if a candidate earns the required credits vide clause 4.4.1, 4.4.2 and 4.4.3 by registering the required number of courses in advance (up to second semester).

4.4.5 A candidate can earn a maximum of 15 credits through all value added courses, online courses and self study courses.

4.5 Flexibility to Add or Drop Courses

4.5.1 A candidate has to earn the total number of credits specified in the curriculum of the respective programme of study in order to be eligible to obtain the degree. However, if the candidate wishes, then the candidate is permitted to earn more than the total number of credits prescribed in the curriculum of the candidate's programme.

4.5.2 From the second to fourth semesters the candidates have the option of registering for additional elective/Honors courses or dropping of already registered additional elective/Honors courses within two weeks from the start of the semester. Add / Drop is only an option given to the candidates. Total number of credits of such courses during the entire programme of study cannot exceed six.

4.6 Maximum number of credits the candidate can enroll in a particular semester cannot exceed 30 credits.

4.7 The blend of different courses shall be so designed that the candidate at the end of the programme would have been trained not only in his / her relevant professional field but also would have developed to become a socially conscious human being.

4.8 The medium of instruction, examinations and project report shall be English.

5. DURATION OF THE PROGRAMME

5.1 A candidate is normally expected to complete the ME / MTech Degree programme in 4 consecutive semesters (2 Years), but in any case not more than 8 semesters (4 Years).

5.2 Each semester shall consist of a minimum of 90 working days including continuous assessment test period. The Head of the Department shall ensure that every teacher imparts instruction as per the number of periods specified in the syllabus for the course being taught.

5.3 The total duration for completion of the programme reckoned from the commencement of the first semester to which the candidate was admitted shall not exceed the maximum duration specified in clause 5.1 irrespective of the period of break of study (vide clause 11) or prevention (vide clause 9) in order that the candidate may be eligible for the award of the degree (vide clause 16). Extension beyond the prescribed period shall not be permitted.

6. COURSE REGISTRATION FOR THE EXAMINATION

6.1 Registration for the end semester examination is mandatory for courses in the current semester as well as for the arrear courses failing which the candidate will not be permitted to move on to the higher semester. This will not be applicable for the courses which do not have an end semester examination.

6.2 The candidates who need to reappear for the courses which have only continuous assessment shall enroll for the same in the subsequent semester, when offered next, and repeat the course. In this case, the candidate shall attend the classes, satisfy the attendance requirements (vide clause 8), earn continuous assessment marks. This will be considered as an attempt for the purpose of classification.

6.3 If a candidate is prevented from writing end semester examination of a course due to lack of attendance, the candidate has to attend the classes, when offered next, and fulfill the attendance requirements as per clause 8 and earn continuous assessment marks. If the course, in which the candidate has a lack of attendance, is an elective, the candidate may register for the same or any other elective course in the subsequent semesters and that will be considered as an attempt for the purpose of classification.

7. ASSESSMENT AND EXAMINATION PROCEDURE FOR AWARDING MARKS

7.1 The ME/MTech programmes consist of Theory Courses, Theory cum Practical courses, Practical courses, Innovative Project, Internship cum Project work and Project Work. Performance in each course of study shall be evaluated based on (i) Continuous Assessments (CA) throughout the semester and (ii) End Semester Examination (ESE) at the end of the semester except for the courses which are evaluated based on continuous assessment only. Each course shall be evaluated for a maximum of 100 marks as shown below:

Sl. No.	Category of Course	Continuous Assessment Marks	End Semester Examination
1.	Theory / Practical	50	50
2.	Theory cum Practical	The distribution of marks shall be decided based on the credit weightage assigned to theory and practical components respectively.	
3.	Innovative Project/ Project Work / Internship cum Project Work	50	50
4.	Value Added Course	The distribution of marks shall be decided based on the credit the credit weightage assigned	---
5.	All other Courses		

7.2 Examiners for setting end semester examination question papers for theory courses, theory cum practical courses and practical courses and evaluating end semester examination answer scripts, project works, innovative project and internships shall be appointed by the Controller of Examinations after obtaining approval from the Principal.

7.3 Theory Courses

For all theory courses out of 100 marks, the continuous assessment shall be 50 marks and the end semester examination shall be for 50 marks. However, the end semester examinations shall be conducted for 100 marks and the marks obtained shall be reduced to 50. The continuous assessment tests shall be conducted as per the schedule laid down in the academic schedule. Three tests shall be conducted for 50 marks each and reduced to 30 marks each. The total of the continuous assessment marks and the end semester examination marks shall be rounded off to the nearest integer.

7.3.1 The assessment pattern for awarding continuous assessment marks shall be as follows:

Sl. No.	Type	Max. Marks	Remarks
1.	Test – I	30	Average of best two
	Test – II	30	
	Test - III	30	
2.	Tutorial	15	Should be of Open Book/Objective Type. Average of best 4 (or more, depending on the nature of the course, as may be approved by Principal)

3.	Assignment / Paper Presentation in Conference / Seminar / Comprehension / Activity based learning / Class notes	05	To be assessed by the Course Teacher based on any one type.
	Total	50	Rounded off to the one decimal place

However, the assessment pattern for awarding the continuous assessment marks may be changed based on the nature of the course and is to be approved by the Principal.

7.3.2 A reassessment test or tutorial covering the respective test or tutorial portions may be conducted for those candidates who were absent with valid reasons (Sports or any other reason approved by the Principal).

7.3.3 The end semester examination for theory courses shall be for duration of three hours.

7.4 Theory cum Practical Courses

For courses involving theory and practical components, the evaluation pattern as per the clause 7.1 shall be followed. Depending on the nature of the course, the end semester examination shall be conducted for theory and the practical components. The apportionment of continuous assessment and end semester examination marks shall be decided based on the credit weightage assigned to theory and practical components approved by Principal.

7.5 Practical Courses

For all practical courses out of 100 marks, the continuous assessment shall be for 50 marks and the end semester examination shall be for 50 marks. Every exercise / experiment shall be evaluated based on the candidate's performance during the practical class and the candidate's records shall be maintained.

7.5.1 The assessment pattern for awarding continuous assessment marks for each course shall be decided by the course coordinator based on rubrics of that particular course, and shall be based on rubrics for each experiment.

7.6 Project Work

7.6.1 Project work shall be carried out individually. Candidates can opt for full time internship (vide clause 7.8) in lieu of project work in third semester. The project work is mandatory for all the candidates.

7.6.2 The Head of the Department shall constitute review committee for project work. There shall be two assessments by the review committee during the semester. The candidate shall make presentation on the progress made by him/her before the committee.

7.6.3 The continuous assessment and end semester examination marks for Project Work and the Viva-Voce Examination shall be distributed as below.

Continuous Assessment (Max. 50 Marks)						End Semester Examination (Max. 50 Marks)			
Review I (Max..10 Marks)		Review II (Max.. 20 Marks)		Review III (Max. 20 Marks)		Report Evaluation (Max. 20 Marks)	Viva - Voce (Max. 30 Marks)		
Rv. Com	Guide	Review Committee (excluding guide)	Guide	Review Committee (excluding guide)	Guide	Ext. Exr.	Guide	Exr. 1	Exr. 2
5	5	10	10	10	10	20	10	10	10

7.6.4 The Project Report prepared according to approved guidelines and duly signed by the Guide and Project Co-ordinator shall be submitted to Head of the Department. A candidate must submit the project report within the specified date as per the academic schedule of the semester. If the project report is not submitted within the specified date then the candidate is deemed to have failed in the Project Work and redo it in the subsequent semester. This applies to both Internship cum Project work and Project work.

7.6.5 If a candidate fails to secure 50% of the continuous assessment marks in the project work, he / she shall not be permitted to submit the report for that particular semester and shall have to redo it in the subsequent semester and satisfy attendance requirements.

7.6.6 Every candidate shall, based on his/her project work, publish a paper in a reputed journal or reputed conference in which full papers are published after usual review. A copy of the full paper accepted and proof for that shall be produced at the time of evaluation.

7.6.7 The project work shall be evaluated based on the project report submitted by the candidate in the respective semester and viva-voce examination by a committee consisting of two examiners and guide of the project work.

7.6.8 If a candidate fails to secure 50 % of the end semester examination marks in the project work, he / she shall be required to resubmit the project report within 30 days from the date of declaration of the results and a fresh viva-voce examination shall be conducted as per clause 7.6.7.

7.6.9 A copy of the approved project report after the successful completion of viva-voce examination shall be kept in the department library.

7.7 Innovative Project

The evaluation method shall be same as that of the Project Work as per clause 7.6 excluding clause 7.6.6.

7.8 Internship cum Project Work

Each candidate shall submit a brief report about the internship undergone and a certificate issued from the organization concerned at the time of Viva-voce examination to the review committee. The evaluation method shall be same as that of the Project Work as per clause 7.6 excluding 7.6.6.

7.9 Value Added Course

Two assessments shall be conducted during the value added course duration by the offering department concerned.

7.10 Online Course

The Board of Studies will provide methodology for the evaluation of the online courses. The Board can decide whether to evaluate the online courses through continuous assessment and end semester examination or through end semester examination only. In case of credits earned through online mode from NPTEL / SWAYAM / a University / Other Agencies approved by Chairman, Academic Council, the credits may be transferred and grades shall be assigned accordingly.

7.11 Self Study Course

The member of faculty approved by the Head of the Department shall be responsible for periodic monitoring and evaluation of the course. The course shall be evaluated through continuous assessment and end semester examination. The evaluation methodology shall be the same as that of a theory course.

7.12 Audit Course

A candidate may be permitted to register for specific course not listed in his/her programme curriculum and without undergoing the rigors of getting a 'good' grade, as an Audit course, subject to the following conditions.

The candidate can register only one Audit course in a semester starting from second semester subject to a maximum of two courses during the entire programme of study. Such courses shall be indicated as 'Audit' during the time of Registration itself. Only courses currently offered for credit to the candidates of other branches can be audited.

A course appearing in the curriculum of a candidate cannot be considered as an audit course. However, if a candidate has already met the Professional Elective and Open Elective credit requirements as stipulated in the curriculum, then, a Professional Elective or an Open Elective course listed in the curriculum and not taken by the candidate for credit can be considered as an audit course.

Candidates registering for an audit course shall meet all the assessment and examination requirements (vide clause 7.3) applicable for a credit candidate of that course. Only if the candidate obtains a performance grade, the course will be listed in the semester Grade Sheet and in the Consolidated Grade Sheet along with the grade SF (Satisfactory). Performance grade will not be shown for the audit course.

Since an audit course has no grade points assigned, it will not be counted for the purpose of GPA and CGPA calculations.

8. REQUIREMENTS FOR COMPLETION OF A SEMESTER

8.1 A candidate who has fulfilled the following conditions shall be deemed to have satisfied the requirements for completion of a semester and permitted to appear for the examinations of that semester.

8.1.1 Ideally, every candidate is expected to attend all classes and secure 100 % attendance. However, a candidate shall secure not less than 80 % (after rounding off to the nearest integer) of the overall attendance taking into account the total number of working days in a semester.

8.1.2 A candidate who could not satisfy the attendance requirements as per clause 8.1.1 due to medical reasons (hospitalization / accident / specific illness) but has secured not less than 70 % in the current semester may be permitted to appear for the current semester examinations with the approval of the Principal on payment of a condonation fee as may be fixed by the authorities from time to time. The medical certificate needs to be submitted along with the leave application. A candidate can avail this provision only twice during the entire duration of the degree programme.

8.1.3 In addition to clause 8.1.1 or 8.1.2, a candidate shall secure not less than 60 % attendance in each course.

8.1.4 A candidate shall be deemed to have completed the requirements of study of any semester only if he/she has satisfied the attendance requirements (vide clause 8.1.1 to 8.1.3) and has registered for examination by paying the prescribed fee.

8.1.5 Candidate's progress is satisfactory.

8.1.6 Candidate's conduct is satisfactory and he/she was not involved in any indisciplined activities in the current semester.

8.2. The candidates who do not complete the semester as per clauses from 8.1.1 to 8.1.6 except 8.1.3 shall not be permitted to appear for the examinations at the end of the semester and not be permitted to go to the next semester. They have to repeat the incomplete semester in next academic year.

8.3 The candidates who satisfy the clause 8.1.1 or 8.1.2 but do not complete the course as per clause 8.1.3 shall not be permitted to appear for the end semester examination of that course alone. They have to repeat the incomplete course in the subsequent semester when it is offered next.

9. REQUIREMENTS FOR APPEARING FOR END SEMESTER EXAMINATION

9.1 A candidate shall normally be permitted to appear for end semester examination of the current semester if he/she has satisfied the semester completion requirements as per clause 8, and has registered for examination in all courses of that semester. Registration is mandatory for current semester examinations as well as for arrear examinations failing which the candidate shall not be permitted to move on to the higher semester.

9.2 When a candidate is deputed for a National / International Sports event during End Semester examination period, supplementary examination shall be conducted for such a candidate on return after participating in the event within a reasonable period of time. Such appearance shall be considered as first appearance.

9.3 A candidate who has already appeared for a course in a semester and passed the examination is not entitled to reappear in the same course for improvement of letter grades / marks.

10. PROVISION FOR WITHDRAWAL FROM EXAMINATIONS

10.1 A candidate may, for valid reasons, be granted permission to withdraw from appearing for the examination in any regular course or all regular courses registered in a particular semester. Application for withdrawal is permitted only once during the entire duration of the degree programme.

10.2 The withdrawal application shall be valid only if the candidate is otherwise eligible to write the examination (vide clause 9) and has applied to the Principal for permission prior to the last examination of that semester after duly recommended by the Head of the Department.

10.3 The withdrawal shall not be considered as an appearance for deciding the eligibility of a candidate for First Class with Distinction/First Class.

10.4 If a candidate withdraws a course or courses from writing end semester examinations, he/she shall register the same in the subsequent semester and write the end semester examinations. A final semester candidate who has withdrawn shall be permitted to appear for supplementary examination to be conducted within reasonable time as per clause 14.

10.5 The final semester candidate who has withdrawn from appearing for project viva-voce for genuine reasons shall be permitted to appear for supplementary viva-voce examination within reasonable time with proper application to Controller of Examinations and on payment of prescribed fee.

11. PROVISION FOR BREAK OF STUDY

11.1 A candidate is normally permitted to avail the authorised break of study under valid reasons (such as accident or hospitalization due to prolonged ill health or any other valid reasons) and to rejoin the programme in a later semester. He/She shall apply in advance to the Principal, through the Head of the Department, stating the reasons therefore, in any case, not later than the last date for registering for that semester examination. A candidate is permitted to avail the authorised break of study only once during the entire period of study for a maximum period of one year. However, in extraordinary situation the candidate may apply for additional break of study not exceeding another one year by paying prescribed fee for the break of study.

11.2 The candidates permitted to rejoin the programme after break of study / prevention due to lack of attendance shall be governed by the rules and regulations in force at the time of rejoining.

11.3 The candidates rejoining in new Regulations shall apply to the Principal in the prescribed format through Head of the Department at the beginning of the readmitted semester itself for prescribing additional/equivalent courses, if any, from any semester of the regulations in-force, so as to bridge the curriculum in-force and the old curriculum.

11.4 The total period of completion of the programme reckoned from the commencement of the semester to which the candidate was admitted shall not exceed the maximum period specified in clause 5 irrespective of the period of break of study in order to qualify for the award of the degree.

11.5 If any candidate is prevented for want of required attendance, the period of prevention shall not be considered as authorized break of study.

11.6 If a candidate has not reported to the college for a period of two consecutive semesters without any intimation, the name of the candidate shall be deleted permanently from the college enrollment. Such candidates are not entitled to seek readmission under any circumstances.

12. PASSING REQUIREMENTS

12.1 A candidate who secures not less than 50 % of total marks (continuous assessment and end semester examination put together) prescribed for the course with a minimum of 50 % of the marks prescribed for the end semester examination in all category of courses vide clause 7.1 except for the courses which are evaluated based on continuous assessment only shall be declared to have successfully passed the course in the examination.

12.2 A candidate who secures not less than 50 % in continuous assessment marks prescribed for the courses which are evaluated based on continuous assessment only shall be declared to have successfully passed the course. If a candidate secures less than 50% in the continuous assessment marks, he / she shall have to re-enroll for the same in the subsequent semester and satisfy the attendance requirements.

12.3 For a candidate who does not satisfy the clause 12.1, the continuous assessment marks secured by the candidate in the first attempt shall be retained and considered valid for subsequent attempts. However, from the fourth attempt onwards the marks scored in the end semester examinations alone shall be considered, in which case the candidate shall secure minimum 50 % marks in the end semester examinations to satisfy the passing requirements, but the grade awarded shall be only the lowest passing grade irrespective of the marks secured.

13. REVALUATION OF ANSWER SCRIPTS

A candidate shall apply for a photocopy of his / her semester examination answer script within a reasonable time from the declaration of results, on payment of a prescribed fee by submitting the proper application to the Controller of Examinations. The answer script shall be pursued and justified jointly by a faculty member who has handled the course and the course coordinator and recommended for revaluation. Based on the recommendation, the candidate can register for revaluation through proper application to the Controller of Examinations. The Controller of Examinations will arrange for revaluation and the results will be intimated to the candidate concerned. Revaluation is permitted only for Theory courses and Theory cum Practical courses where end semester examination is involved.

14. SUPPLEMENTARY EXAMINATION

If a candidate fails to clear all courses in the final semester after the announcement of final end semester examination results, he/she shall be allowed to take up supplementary examinations to be conducted within a reasonable time for the courses of final semester alone, so that he/she gets a chance to complete the programme.

15. AWARD OF LETTER GRADES

Range of % of Total Marks	Letter Grade	Grade Point
91 to 100	O (Outstanding)	10
81 to 90	A+ (Excellent)	9
71 to 80	A (Very Good)	8
61 to 70	B+ (Good)	7
50 to 60	B (Average)	6
Less than 50	RA (Reappear)	0
Satisfactory	SF	0
Withdrawal	W	-
Absent	AB	-
Shortage of Attendance in a course	SA	-

The Grade Point Average (GPA) is calculated using the formula:

$$GPA = \frac{\sum[(\text{course credits}) \times (\text{grade points})] \text{ for all courses in the specific semester}}{\sum(\text{course credits}) \text{for all courses in the specific semester}}$$

The Cumulative Grade Point Average (CGPA) is calculated from first semester (third semester for lateral entry candidates) to final semester using the formula

$$CGPA = \frac{\sum[(\text{course credits}) \times (\text{grade points})] \text{ for all courses in all the semesters so far}}{\sum(\text{course credits}) \text{for all courses in all the semesters so far}}$$

The GPA and CGPA are computed only for the candidates with a pass in all the courses.

The GPA and CGPA indicate the academic performance of a candidate at the end of a semester and at the end of successive semesters respectively.

A grade sheet for each semester shall be issued containing Grade obtained in each course, GPA and CGPA.

A duplicate copy, if required can be obtained on payment of a prescribed fee and satisfying other procedure requirements.

Withholding of Grades: The grades of a candidate may be withheld if he/she has not cleared his/her dues or if there is a disciplinary case pending against him/her or for any other reason.

16. ELIGIBILITY FOR THE AWARD OF DEGREE

A candidate shall be declared to be eligible for the award of the ME / MTech Degree provided the candidate has

i. Successfully completed all the courses under the different categories, as specified in the regulations.

ii. Successfully gained the required number of total credits as specified in the curriculum corresponding to the candidate's programme within the stipulated time (vide clause 5).

iii. Successfully passed any additional courses prescribed by the respective Board of Studies whenever readmitted under regulations other than R-2020 (vide clause 11.3)

iv. No disciplinary action pending against him / her.

17. CLASSIFICATION OF THE DEGREE AWARDED

17.1 First Class with Distinction:

17.1.1 A candidate who qualifies for the award of the degree (vide clause 16) and who satisfies the following conditions shall be declared to have passed the examination in First class with Distinction:

- Should have passed the examination in all the courses of all the four semesters in the **First Appearance** within four consecutive semesters excluding the authorized break of study (vide clause 11) after the commencement of his / her study.

- Withdrawal from examination (vide clause 10) shall not be considered as an appearance.
- Should have secured a CGPA of not less than 8.50

(OR)

17.1.2 A candidate who joins from other institutions on transfer or a candidate who gets readmitted and has to move from one regulation to another regulation and who qualifies for the award of the degree (vide clause 16) and satisfies the following conditions shall be declared to have passed the examination in First class with Distinction:

- Should have passed the examination in all the courses of all the four semesters in the **First Appearance** within four consecutive semesters excluding the authorized break of study (vide clause 11) after the commencement of his / her study.
- Submission of equivalent course list approved by the respective Board of studies.
- Withdrawal from examination (vide clause 10) shall not be considered as an appearance.
- Should have secured a CGPA of not less than 9.00

17.2 First Class:

A candidate who qualifies for the award of the degree (vide clause 16) and who satisfies the following conditions shall be declared to have passed the examination in First class:

- Should have passed the examination in all the courses of all four semesters within six consecutive semesters excluding authorized break of study (vide clause 11) after the commencement of his / her study.
- Withdrawal from the examination (vide clause 10) shall not be considered as an appearance.
- Should have secured a CGPA of not less than 7.00

17.3 Second Class:

All other candidates (not covered in clauses 17.1 and 17.2) who qualify for the award of the degree (vide clause 16) shall be declared to have passed the examination in Second Class.

17.4 A candidate who is absent for end semester examination in a course / project work after having registered for the same shall be considered to have appeared for that examination for the purpose of classification.

18. MALPRACTICES IN TESTS AND EXAMINATIONS

If a candidate indulges in malpractice in any of the tests or end semester examinations, he/she shall be liable for punitive action as per the examination rules prescribed by the college from time to time.

19. AMENDMENTS

Notwithstanding anything contained in this manual, the Kongu Engineering College through the Academic council of the Kongu Engineering College, reserves the right to modify/amend without notice, the Regulations, Curricula, Syllabi, Scheme of Examinations, procedures, requirements, and rules pertaining to its ME / MTech programme.

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CURRICULUM BREAKDOWN STRUCTURE						
Summary of Credit Distribution						
Category	**Semester**				**Total number of credits**	**Curriculum Content (% of total number of credits of the program)**
	I	**II**	**III**	**IV**		
FC	**7**	**-**	**-**	**-**	**7**	**9.72**
PC	**13**	**14**	**-**	**-**	**27**	**37.50**
PE	**3**	**6**	**3**	**6**	**18**	**25.00**
EC		**2**	**9**	**9**	**20**	**27.78**
Semester wise Total	**23**	**22**	**12**	**15**	**72**	**100.00**

Category	Abbreviation
Lecture hours per week	**L**
Tutorial hours per week	**T**
Practical, Project work, Internship, Professional Skill Training, Industrial Training hours per week	**P**
Credits	**C**

CATEGORISATION OF COURSES							
FOUNDATION COURSES (FC)							
S. No.	**Course Code**	**Course Name**	**L**	**T**	**P**	**C**	**Sem**
1.	20AMT13	Applied Mathematics for Electronics Engineers	3	1	0	4	1
2.	20GET11	Introduction to Research	2	1	0	3	1
Total Credits to be earned						7	
PROFESSIONAL CORE (PC)							
S. No.	**Course Code**	**Course Name**	**L**	**T**	**P**	**C**	**Sem**
1.	20EST11	Programming Languages for Embedded Systems	3	1	0	4	1
2.	20EST12	Microcontroller System Design	3	0	0	3	1
3.	20EST13	Advanced Digital System Design	3	1	0	4	1
4.	20ESL11	Microcontroller System Design Laboratory	0	0	2	1	1
5.	20ESL12	Programming Languages for Embedded Systems Laboratory	0	0	2	1	1
6.	20EST21	Embedded Networking and Buses	3	0	0	3	2
7.	20EST22	RTOS for Embedded System	3	1	0	4	2

8.	20EST23	Design of Embedded Systems	3	0	0	3	2
9.	20EST24	Embedded Linux	2	0	2	3	2
10.	20ESL21	Embedded Networking and Buses Laboratory	0	0	2	1	2
Total Credits to be earned						27	
PROFESSIONAL ELECTIVE (PE)							
S. No.	**Course Code**	**Course Name**	**L**	**T**	**P**	**C**	**Sem**
		Elective 1					
1.	20ESE01	Distributed Embedded Computing	3	0	0	3	1
2.	20ESE02	Solar and Energy Storage System	3	0	0	3	1
3.	20ESE03	Semiconductor Memory Design	3	0	0	3	1
4.	20ESE21	Testing of VLSI Circuits	3	0	0	3	1
		Elective 2					
5.	20ESE04	QT Cross Compiling Application Development	3	0	0	3	2
6.	20ESE05	Sensors and Actuators for Robotics	3	0	0	3	2
7.	20ESE06	Verilog HDL for Embedded FPGA processor	3	0	0	3	2
		Elective 3					
8.	20ESE07	Computer Based Industrial Control	3	0	0	3	2
9.	20ESE08	RISC processor	3	0	0	3	2
10.	20ESE09	Design of Embedded Control System	3	0	0	3	2
11.	20ESE22	Application Specific Integrated Circuits	2	0	2	3	2
		Elective 4					
12.	20ESE10	Nature Inspired Optimization Technique	3	0	0	3	3
13.	20ESE11	Supervised Machine Learning Algorithm	3	0	0	3	3
14.	20ESE12	Signal and Image Processing for Real Time Applications	3	0	0	3	3
15.	20ESE23	Low Power VLSI Design	3	0	0	3	3
		Elective 5					
16.	20ESE13	Programming Internet of Things	3	0	0	3	4
17.	20ESE14	Single Board Computer	3	0	0	3	4
18.	20ESE15	System on Chip for Embedded Applications	3	0	0	3	4
19.	20ESE16	Sensors and Engine Management System	3	0	0	3	4
20.	20ESE24	Computer Aided Design of VLSI Circuits	3	0	0	3	4

		Elective 6					
21.	20ESE17	Multicore Processor and Computing	3	0	0	3	4
22.	20ESE18	DSP Processor Architecture and Programming	3	0	0	3	4
23.	20ESE19	Design and Analysis of Algorithms	3	0	0	3	4
24.	20ESE20	Virtual Instrumentation for Industrial Applications	3	0	0	3	4
25.	20GET13	Innovation, Entrepreneurship and Venture Development	3	0	0	3	4
Total Credits to be earned						18	
EMPLOYABILITY ENHANCEMENT COURSES (EC)							
S. No.	**Course Code**	**Course Name**	**L**	**T**	**P**	**C**	**Sem**
1.	20ESP21	Innovative Project	0	0	4	2	2
2.	20ESP31	Internship cum Project Work	0	0	18	9	3
3.	20ESP41	Project Work	0	0	18	9	4
Total Credits to be earned						20	

KEC R2020: SCHEDULING OF COURSES – ME (Embedded Systems) Total Credits : 72

Sem	Course1	Course2	Course3	Course4	Course5	Course6	Course7	Course8	Credits
I	20GET11 Introduction to Research (PC-2-1-0-3)	20AMT13 Applied Mathematics for Electronics Engineers (FC-3-1-0-4)	20EST11 Programming Languages for Embedded Systems (PC-3-1-0-4)	20EST12 Microcontroller System Design (PC-3-0-0-3)	20EST13 Advanced Digital System Design (PC-3-1-0-4)	20ESL11 Microcontroller System Design laboratory (PC-0-0-2-1)	20ESL12 Programming Languages for Embedded Systems Laboratory (PC-0-0-2-1)	Professional Elective I (PE-3-0-0-3)	**23**
II	20EST21 Embedded Networking and Buses (PC-3-0-0-3)	20EST22 RTOS for Embedded System (PC-3-1-0-4)	20EST23 Design of Embedded Systems (PC-3-0-0-3)	20EST24 Embedded Linux (PC-2-0-2-3)	Professional Elective II (PE-3-0-0-3)	Professional Elective III (PE-3-0-0-3)	20ESL21 Embedded Networking and Buses Laboratory (PC-0-0-2-1)	20ESP21 Innovative Project (EC-0-0-4-2)	**22**
III	Professional Elective IV (PE-3-0-0-3)	20ESP31 Industrial Project (EC-0-0-18-9)							**12**
IV	Professional Elective V (PE-3-0-0-3)	Professional Elective VI (PE-3-0-0-3)	20ESP41 Project work (EC-0-0-18-9)						**15**

MAPPING OF COURSES WITH PROGRAM OUTCOMES

Sem.	Course Code	Course Title	PO1	PO2	PO3	PO4	PO5	PO6
1	20MAT13	Applied Mathematics for Electronics Engineers	✓		✓	✓	✓	
1	20GET11	Introduction to Research	✓	✓	✓			
1	20EST11	Programming Languages for Embedded Systems	✓	✓	✓	✓	✓	✓
1	20EST12	Microcontroller System Design	✓	✓	✓	✓	✓	✓
1	20EST13	Advanced Digital System Design	✓	✓	✓	✓	✓	
1	20ESL11	Microcontroller System Design Laboratory	✓	✓	✓	✓	✓	✓
1	20ESL12	Programming Languages for Embedded Systems Laboratory	✓	✓	✓	✓	✓	
2	20EST21	Embedded Networking and Buses	✓		✓	✓		✓
2	20EST22	RTOS for Embedded System	✓	✓	✓	✓	✓	✓
2	20EST23	Design of Embedded Systems	✓		✓	✓	✓	✓
2	20ESE24	Embedded Linux	✓	✓	✓	✓	✓	
2	20ESL21	Embedded Networking and Buses Laboratory	✓	✓	✓	✓	✓	
2	20ESP21	Innovative Project	✓	✓	✓	✓	✓	✓
3	20ESP31	Internship cum Project Work	✓	✓	✓	✓	✓	✓
4	20ESP41	Project Work	✓	✓	✓	✓	✓	✓
		Professional Elective Courses						
1	20ESE01	Distributed Embedded Computing	✓	✓	✓	✓		
1	20ESE02	Solar and Energy Storage System	✓		✓	✓		✓
1	20ESE03	Semiconductor Memory Design	✓		✓	✓		
2	20ESE04	QT Cross Compiling Application Development	✓		✓	✓	✓	✓
2	20ESE05	Sensors and Actuators for Robotics	✓		✓	✓	✓	✓
2	20ESE06	Verilog HDL for Embedded FPGA processor	✓		✓	✓	✓	
2	20ESE07	Computer Based Industrial Control	✓		✓	✓	✓	✓
2	20ESE08	RISC processor	✓		✓	✓	✓	✓

2	20ESE09	Design of Embedded Control System	✓		✓	✓		
3	20ESE10	Nature Inspired Optimization Technique	✓		✓	✓		✓
3	20ESE11	Supervised Machine Learning Algorithm	✓	✓	✓		✓	
3	20ESE12	Signal and Image Processing for Real Time Applications	✓		✓	✓		
4	20ESE13	Programming Internet of Things	✓	✓	✓	✓	✓	✓
4	20ESE14	Single Board Computer	✓	✓	✓	✓	✓	✓
4	20ESE15	System on Chip for Embedded Applications	✓		✓	✓		✓
4	20ESE16	Sensors and Engine Management System	✓	✓	✓	✓		
4	20ESE17	Multicore Processor and Computing	✓	✓	✓	✓	✓	✓
4	20ESE18	DSP Processor Architecture and Programming	✓	✓	✓	✓	✓	✓
4	20ESE19	Design and Analysis of Algorithms	✓	✓	✓	✓	✓	✓
4	20ESE20	Virtual Instrumentation for Industrial Applications	✓	✓	✓	✓	✓	✓
4	20GET13	Innovation, Entrepreneurship and Venture Development	✓	✓	✓	✓	✓	✓
1	20ESE21	Testing of VLSI Circuits			✓		✓	
2	20ESE22	Application Specific Integrated Circuits	✓	✓	✓	✓	✓	✓
3	20ESE23	Low Power VLSI Design	✓	✓	✓	✓	✓	✓
4	20ESE24	Computer Aided Design of VLSI Circuits	✓	✓	✓	✓	✓	✓

M.E. EMBEDDED SYSTEMS CURRICULUM-R2020

SEMESTER – I									
Course Code	Course Title	Hours / Week			Credit	Maximum Marks			Category
		L	T	P		CA	ESE	Total	
THEORY									
20GET11	Introduction to Research	2	1	0	3	50	50	100	FC
20AMT13	Applied Mathematics for Electronics Engineers	3	1	0	4	50	50	100	FC
20EST11	Programming Languages for Embedded Systems	3	1	0	4	50	50	100	PC
20EST12	Microcontroller System Design	3	0	0	3	50	50	100	PC
20EST13	Advanced Digital System Design	3	1	0	4	50	50	100	PC
	Professional Elective - I	3	0	0	3	50	50	100	PE
Practical / Employability Enhancement									
20ESL11	Microcontroller System Design Laboratory	0	0	2	1	50	50	100	PC
20ESL12	Programming Languages for Embedded Systems Laboratory	0	0	2	1	50	50	100	PC
Total Credits to be earned					**23**				

SEMESTER – II									
Course Code	Course Title	Hours / Week			Credit	Maximum Marks			Category
		L	T	P		CA	ESE	Total	
THEORY									
20EST21	Embedded Networking and Buses	3	0	0	3	50	50	100	PC
20EST22	RTOS for Embedded System	3	1	0	4	50	50	100	PC
20EST23	Design of Embedded Systems	3	0	0	3	50	50	100	PC
20EST24	Embedded Linux	2	0	2	3	50	50	100	PC
	Professional Elective - II	3	0	0	3	50	50	100	PE
	Professional Elective - III	3	0	0	3	50	50	100	PE
Practical / Employability Enhancement									
20ESL21	Embedded Networking and Buses Laboratory	0	0	2	1	50	50	100	PC
20ESP21	Innovative Project	0	0	4	2	50	50	100	EC
Total Credits to be earned					**22**				

SEMESTER – III									
Course Code	Course Title	Hours / Week			Credit	Maximum Marks			Category
		L	T	P		CA	ESE	Total	
Practical / Employability Enhancement									
	Professional Elective - IV	3	0	0	3	50	50	100	PE
20ESP31	Internship cum Project Work	0	0	18	9	50	50	100	EC
Total Credits to be earned					**12**				

SEMESTER – IV									
Course Code	Course Title	Hours / Week			Credit	Maximum Marks			Category
		L	T	P		CA	ESE	Total	
THEORY/THEORY WITH PRACTICAL									
	Professional Elective - V	3	0	0	3	50	50	100	PE
	Professional Elective - VI	3	0	0	3	50	50	100	PE
PRACTICAL									
20ESP41	Project Work	0	0	18	9	50	50	100	EC
Total Credits to be earned					**15**				

LIST OF PROFESSIONAL ELECTIVE COURSES

S. No.	Course Code	Course Name	L	T	P	C
		Semester 1				
		Elective 1				
1.	20ESE01	Distributed Embedded Computing	3	0	0	3
2.	20ESE02	Solar and Energy Storage System	3	0	0	3
3.	20ESE03	Semiconductor Memory Design	3	0	0	3
4	20ESE21	Testing of VLSI Circuits	3	0	0	3
		Semester 2				
		Elective 2				
5.	20ESE04	QT Cross Compiling Application Development	3	0	0	3
6.	20ESE05	Sensors and Actuators For Robotics	3	0	0	3
7.	20ESE06	Verilog HDL for Embedded FPGA processor	3	0	0	3
		Elective 3				
8.	20ESE07	Computer Based Industrial Control	3	0	0	3
9.	20ESE08	RISC processor	3	0	0	3
10.	20ESE09	Design of Embedded Control System	3	0	0	3
11.	20ESE22	Application Specific Integrated Circuits	2	0	2	3
		Semester 3				
		Elective 4				
12.	20ESE10	Nature Inspired Optimization Technique	3	0	0	3
13.	20ESE11	Supervised Machine Learning Algorithm	3	0	0	3
14.	20ESE12	Signal and Image Processing for Real Time Applications	3	0	0	3
15.	20ESE23	Low Power VLSI Design	3	0	0	3
		Semester 4				
		Elective 5				
16.	20ESE13	Programming Internet of Things	3	0	0	3
17.	20ESE14	Single Board Computer	3	0	0	3
18.	20ESE15	System on Chip for Embedded Applications	3	0	0	3
19.	20ESE16	Sensors and Engine Management System	3	0	0	3
20.	20ESE24	Computer Aided Design of VLSI Circuits	3	0	0	3
		Elective 6				
21.	20ESE17	Multicore Processor and Computing	3	0	0	3
22.	20ESE18	DSP Processor Architecture and Programming	3	0	0	3
23.	20ESE19	Design and Analysis of Algorithms	3	0	0	3
24.	20ESE20	Virtual Instrumentation for Industrial Applications	3	0	0	3
25.	20GET13	Innovation, Entrepreneurship and Venture Development	3	0	0	3

20GET11 INTRODUCTION TO RESEARCH

(Common to Engineering and Technology Branches)

Programme & Branch	M.E.- Embedded Systems	Sem.	Category	L	T	P	Credit
Prerequisites	Nil	1	FC	2	1	0	3

Preamble	Preamble: This course will familiarize the fundamental concepts/techniques adopted in research, problem formulation and patenting. Also will disseminate the process involved in collection, consolidation of published literature and rewriting them in a presentable form using latest tools.	
Unit - I	**Concept of Research**	**6+3**
Meaning and Significance of Research: Skills, Habits and Attitudes for Research - Time Management - Status of Research in India. Why, How and What a Research is? - Types and Process of Research - Outcome of Research - Sources of Research Problem - Characteristics of a Good Research Problem - Errors in Selecting a Research Problem - Importance of Keywords - Literature Collection – Analysis - Citation Study - Gap Analysis - Problem Formulation Techniques.		
Unit - II	**Research Methods and Journals**	**6+3**
Interdisciplinary Research - Need for Experimental Investigations - Data Collection Methods - Appropriate Choice of Algorithms / Methodologies / Methods - Measurement and Result Analysis - Investigation of Solutions for Research Problem - Interpretation - Research Limitations. Journals in Science/Engineering - Indexing and Impact factor of Journals - Citations - h Index - i10 Index - Journal Policies - How to Read a Published Paper - Ethical issues Related to Publishing - Plagiarism and Self-Plagiarism.		
Unit - III	**Paper Writing and Research Tools**	**6+3**
Types of Research Papers - Original Article/Review Paper/Short Communication/Case Study - When and Where to Publish? - Journal Selection Methods. Layout of a Research Paper - Guidelines for Submitting the Research Paper - Review Process - Addressing Reviewer Comments. Use of tools / Techniques for Research - Hands on Training related to Reference Management Software - EndNote, Software for Paper Formatting like LaTeX/MS Office. Introduction to Origin, SPSS, ANOVA etc., Software for detection of Plagiarism.		
Unit - IV	**Effective Technical Thesis Writing/Presentation**	**6+3**
How to Write a Report - Language and Style - Format of Project Report - Use of Quotations - Method of Transcription Special Elements: Title Page - Abstract - Table of Contents - Headings and Sub-Headings - Footnotes - Tables and Figures - Appendix - Bibliography etc. - Different Reference Formats. Presentation using PPTs.		
Unit - V	**Nature of Intellectual Property**	**6+3**
Patents - Designs - Trade and Copyright. Process of Patenting and Development: Technological research - innovation - patenting - development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents.		

Lecture: 30, Tutorial:15, Total:45

REFERENCES:

1	DePoy, Elizabeth, and Laura N. Gitlin, “Introduction to Research-E-Book: Understanding and Applying Multiple Strategies”, Elsevier Health Sciences, 2015.
2	Walliman, Nicholas, “Research Methods: The basics”,Routledge, 2017.
3.	Bettig Ronald V., “Copyrighting culture: The political economy of intellectual property”,Routledge, 2018.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	list the various stages in research and categorize the quality of journals.	Analyzing (K4)
CO2	formulate a research problem from published literature/journal papers	Evaluating (K5)
CO3	write, present a journal paper/ project report in proper format	Creating (K6)
CO4	select suitable journal and submit a research paper.	Applying (K3)
CO5	compile a research report and the presentation	Applying (K3)

Mapping of COs with POs and PSOs					
COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**
CO1	3	2	1		
CO2	3	2	3		
CO3	3	3	1		
CO4	3	2	1		
CO5	3	2	1		
1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy					

ASSESSMENT PATTERN - THEORY							
Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1		30	40	30			100
CAT2		30	40	30			100
CAT3			30	40	30		100
ESE		30	40	30			100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

20AMT13 APPLIED MATHEMATICS FOR ELECTRONIC ENGINEERS

(Common to VLSI Design and Embedded Systems)

Programme & Branch	M.E.- Embedded Systems	Sem.	Category	L	T	P	Credit
Prerequisites	NIL	1	FC	3	1	0	4

Preamble	This course will demonstrate various analytical skills in applied mathematics and use extensive mathematical tools such as linear programming, matrix factorizations and queuing theory with the tactics of problem solving and logical thinking applicable in electronics engineering.	
Unit - I	**Advanced Matrix Theory**:	**9+3**
Positive definite matrices – Cholesky decomposition – Generalized Eigenvectors – Canonical basis – QR factorization – Generalized inverses – Singular value decomposition – Least squares solution.		
Unit - II	**Vector Spaces:**	**9+3**
Definition – Subspaces – Linear dependence and independence – Basis and dimension – Row space, Column space and Null Space – Rank and nullity.		
Unit - III	**Linear Programming:**	**9+3**
Mathematical Formulation of LPP – Basic definitions – Solutions of LPP: Graphical method – Simplex method – Transportation Model – Mathematical Formulation – Initial Basic Feasible Solution: North west corner rule – Vogel's approximation method – Optimum solution by MODI method – Assignment Model – Mathematical Formulation – Hungarian algorithm.		
Unit - IV	**Non-Linear Programming**	**9+3**
Formulation of non–linear programming problem – Constrained optimization with equality constraints – Constrained optimization with inequality constraints – Graphical method of non–linear programming problem involving only two variables.		
Unit - V	**Queuing Theory:**	**9+3**
Markovian queues – Single and Multi-server Models – Little's formula – Non- Markovian Queues – Pollaczek Khintchine Formula.		

Lecture:45, Practical:15, Total:60

REFERENCES:

1	Bronson, R., "Matrix Operations", Schaum's Outline Series, McGraw Hill, 2011.
2	Howard Anton, "Elementary Linear Algebra" 10th edition, John Wiley & Sons, 2010.
3	Kanti Swarup, Gupta, P.K and Man Mohan "Operations Research", S.Chand & Co., 1997.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	apply various methods in matrix theory to solve system of linear equations.	Applying (K3)
CO2	apply the concepts of linear algebra to solve practical problems.	Applying (K3)
CO3	formulate mathematical models for linear programming problems and solve the transportation and assignment problems.	Applying (K3)
CO4	use non-linear programming concepts in real life situations.	Applying (K3)
CO5	identify the suitable queuing model to handle communication problems.	Applying (K3)

Mapping of COs with POs						
COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	3					
CO2	3					
CO3	3				2	
CO4	3		3	3	2	
CO5	3			3		
1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy						

ASSESSMENT PATTERN - THEORY							
Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	10	20	70	-	-	-	100
CAT2	10	20	70	-	-	-	100
CAT3	10	20	70	-	-	-	100
ESE	10	20	70	-	-	-	100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

20EST11 PROGRAMMING LANGUAGE FOR EMBEDDED SYSTEMS

Programme & Branch	M.E-Embedded Systems	Sem.	Category	L	T	P	Credit
Prerequisites	NIL	**1**	**PC**	**3**	**1**	**0**	**4**

Preamble	To know about the major programming paradigms, the principles and techniques involved in embedded system design and to implement modern programming languages.	
Unit - I	**Introduction to C Language:**	**9+3**
Overview of C-Constants, Variables, and Data types-Operators and Expressions-Managing Input and Output Operations-Decision Making and Branching-Decision Making and Looping-Arrays.		
Unit - II	**C Programming** :	**9+3**
Character Arrays and Strings-User defined Functions-Structures and Unions-Pointers-File Management in C-Dynamic memory allocation and Linked Lists-The Preprocessor.		
Unit - III	**C++ Programming** :	**9+3**
Basics of C++ Programming-Memory models and Namespace-objects and classes-working with classes-classes and dynamic memory allocation-class inheritance-Reusing code in C++-Friends, Exceptions, RTI, and type cast-String class-Input, Output and Files.		
Unit - IV	**Introduction to Python:**	**9+3**
Basics of Python Programming-Decision control statements-Functions and Modules-Python strings-File handling.		
Unit - V	**Advanced topics in Python** :	**9+3**
Classes and objects-Inheritance-Operator overloading-Error and Exception handling.		

Lecture:45, Tutorial:15, Total:60

REFERENCES:

1	Brain W.Kernighan, Dennis Ritche, “The C Programming Language”, 2nd Edition, Pearson, 2015.
2	Reema Thareja, "Python Programming using problem solving approach", 1st Edition, Oxford Publication, 2017.
3	Stanley B. Lippman, Josee Lajoie, Barbara E. Moo, "C++ Primer", 5th Edition, Pearson Education, 2013.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	write programs for data manipulation, I/O process and numerical conversions using C	Applying(K3)
CO2	apply advanced data structures for problem solving	Applying(K3)
CO3	apply python programming concepts for data manipulation	Applying(K3)
CO4	write python programs with object oriented and exception handling features	Applying(K3)
CO5	differentiate interpreted language(Python) from compiled languages(C, C++)	Analyzing(K4)

Mapping of COs with POs						
COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	1	2	2	3	2	
CO2	1	2	2	3	2	
CO3	1	2	3	2	2	
CO4	1	2	3	2	2	
CO5			3	2		1
1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy						

ASSESSMENT PATTERN - THEORY							
Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	10	20	70				100
CAT2		30	70				100
CAT3		10	45	45			100
ESE	10	20	50	20			100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

20EST12 MICROCONTROLLER SYSTEM DESIGN

Programme & Branch	M.E-Embedded Systems	Sem.	Category	L	T	P	Credit
Prerequisites	NIL	**1**	**PC**	**3**	**0**	**0**	**3**

Preamble	To expertise assembly level and C level program for the basic 8051 and PIC18Fxxx microcontroller architecture and able to interface sensors and motors for project development	
Unit - I	**8051 Architecture:**	**9**
Architecture - memory organization - addressing modes - instruction set - timers –counters- Interrupts -I/O ports - Serial Communication.		
Unit - II	**8051 Programming:**	**9**
Assembly language programming - Timer Counter Programming - Serial Communication Programming - Interrupt Programming - Interfacing I/O Devices- RTOS for 8051 – RTOSLite – FullRTOS - Task creation and Run - LCD digital clock/thermometer using FullRTOS		
Unit - III	**PIC Microcontroller** :	**9**
Architecture of PIC18FXX - memory organization - addressing modes - instruction set - I/O port-Simple Assembly Language Programming –Introduction to Embedded C		
Unit - IV	**Peripheral of PIC Microcontroller & programming:**	**9**
I/O Port-Timers - I2C bus-A/D converter-UART-CCP modules -Interrupts -EEPROM memories		
Unit - V	**Hardware interfacing:**	**9**
LCD Display -touch screen- Keypad - SPI Bus Protocol -DS1307 RTC- DC Motor Direction and Speed control using PWM -Stepper Motor		

Lecture:45, Total:45

REFERENCES:

1	Muhammad Ali Mazidi, Janice G. mazidi and Rolin D McKinlay, The 8051 Microcontroller and Embedded Systems, 2nd edition, Prentice Hall, 2014.
2	Muhammad Ali Mazidi, Rolin D McKinlay, Danny Causy, PIC Microcontroller and Embedded Systems using Assembly and C for PIC18, 2nd edition, Pearson Education, 2009.
3	John lovine, PIC Microcontroller Project Book, 2nd edition, McGraw Hill, New Delhi, 2004.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	comprehend the architecture of 8051 and write assembly language program for arithmetic and logical operations	Understanding(K2)
CO2	write assembly language program for internal peripherals of 8051 microcontroller using proteus simulator	Applying(K3)
CO3	demonstrate the concepts of RTOS for 8051 microcontroller	Analyzing(K4)
CO4	write ASM/ C programs to manipulate the peripherials of PIC18Fxx	Applying(K3)
CO5	design a mini Project using DS1307 RTC/DC Motor/Stepper Motor and other I/O devives	Creating(K5)

Mapping of COs with POs						
COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1		2	3	2		
CO2			3	3	2	
CO3	1		3	2		
CO4	2	2	3	2	2	
CO5	3	3	2	3	2	2
1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy						

ASSESSMENT PATTERN - THEORY							
Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	10	60	30				100
CAT2	-	50	30	20			100
CAT3	-	20	40	10		30	100
ESE	10	25	40	10		15	100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

20EST13 ADVANCED DIGITAL SYSTEM DESIGN

Programme & Branch	M.E.- Embedded Systems	Sem.	Category	L	T	P	Credit
Prerequisites	NIL	1	PC	3	1	0	4

Preamble	To design and analyze synchronous, asynchronous digital circuits and to introduce ASM and the architectures of PLD	
Unit - I	**Synchronous Sequential Circuit Design:**	**9+3**
Analysis of Clocked Synchronous Sequential Networks (CSSN)- Modeling of CSSN – State table Reduction- Stable Assignment – Complete Design of CSSN – Design of Iterative Circuits		
Unit - II	**Algorithmic State Machine (ASM):**	**9+3**
ASM-ASM Chart – Synchronous Sequential Network Design Using ASM Charts- State Assignment- ASM Tables-ASM Realization- Asynchronous Inputs.		
Unit - III	**Asynchronous Circuit Design:**	**9+3**
Analysis of Asynchronous Sequential Circuit (ASC) – Flow Table Reduction – Races in ASC – State Assignment – Problem and the Transition Table – Design of ASC – Static and Dynamic Hazards – Essential Hazards		
Unit - IV	**Programming Logic Arrays:**	**9+3**
PLA minimization – Essential Prime Cube theorem- PLA folding- foldable compatibility matrix- The Compact Algorithm. Practical PLA's –Data Synchronizers – Designing Vending Machine Controller – Mixed Operating Mode Asynchronous Circuits		
Unit - V	**Programmable Devices:**	**9+3**
Programmable Logic Devices – Designing a Synchronous Sequential Circuit using a PAL – Realization State machine using PLD – Complex Programmable Logic Devices (CPLDs) – FPGA – Actel ACT.		

Lecture:45, Tutorial:15, Total:60

REFERENCES:

1	Givone Donald G., "Digital Principles and Design", Tata McGraw-Hill, New Delhi, 2008
2	Biswas Nripendra N, "Logic Design Theory", Prentice Hall of India, New Delhi, 2001
3	Yarbrough, John M., "Digital Logic Applications and Design", Thomson Learning, Singapore, 2001.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	design clocked synchronous sequential circuits using state table reduction and assignment	Applying(K3)
CO2	realize the algorithmic state machine using state tables, charts and state assignment	Applying(K3)
CO3	analyze the asynchronous sequential circuit using flow table reduction and find the hazards in circuits	Analyzing(K4)
CO4	simplify the circuits using Programmable logic array, essential cube theorem and compact algorithm	Applying(K3)
CO5	design the synchronous sequential circuits using Programmable Logic Device, Programmable Array Logic and CPLD	Creating(K6)

Mapping of COs with POs and PSOs						
COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	3	3	2		3	
CO2	3	3	2		2	
CO3	3	3	2	1	3	
CO4	3	3	2	1	3	
CO5	3	3	2	1	3	
1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy						

ASSESSMENT PATTERN - THEORY							
Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	5	15	80				100
CAT2	5	15	70	10			100
CAT3		10	60	20		10	100
ESE	5	15	55	15		10	100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

20ESL11 MICROCONTROLLER SYSTEM DESIGN LABORATORY

Programme & Branch	M.E.- Embedded Systems	Sem.	Category	L	T	P	Credit
Prerequisites	NIL	1	PC	0	0	2	1
Preamble	To impart the knowledge of design and development of embedded products using Microcontroller						

List of Exercises / Experiments :

1.	Simulation and implementation of Switch/ Keypad and LED using 89c51 Microcontroller
2.	Simulation and implementation of device ON / OFF using 89c51 microcontroller (Relay and LED)
3.	Simulation and implementation of LCD
4.	Simulation and implementation of 7 segment/ widget display using 89c51 microcontroller
5.	Simulation and implementation of motor –speed and direction using 89c51 microcontroller i)Stepper Motor ii) DC Motor
6.	Interrupt programming using 89c51 microcontroller.
7.	Serial Communication using PIC18F45x microcontroller
8.	Simulation and implementation of Real Time Clock using PIC18F45x microcontroller
9.	Programs for timers using PIC18F45x microcontroller.
10.	PWM / GPS generation using PIC18F45x microcontroller.
11.	I2C / Bluetooth communication using PIC18F45x microcontroller.
12.	Interrupt /GSM programming using PIC18F45x microcontroller

Total: 30

REFERENCES/MANUAL/SOFTWARE:

1.	Proteus Professional
2.	CCS Compiler, UMPS

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	program an 8-bit microcontroller	Applying(K3), Precision(S3)
CO2	write embedded C program for interrupt, ADC , Serial communication and sensor interfacing using CCS compiler	Applying (K3), Precision (S3)
CO3	design and develop embedded based projects and products	Applying (K3), Precision(S3)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1	2	3	3	1	
CO2	2	2	3	3	1	
CO3	3	3	3	3	2	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

20ESL12-PROGRAMMING LANGUAGES FOR EMBEDDED SYSTEMS LABORATORY

Programme & Branch	M.E.- Embedded Systems	Sem.	Category	L	T	P	Credit
Prerequisites	NIL	1	PC	0	0	2	1
Preamble	To impart the knowledge of Programming languages and differentiate interpreted language(Python) from compiled languages(C, C++)						

List of Exercises / Experiments :

1.	C Program demonstrating multi dimensional arrays and functions
2.	C Program demonstrating pointers and file management operations
3.	Implementation of singly linked list and its operations using C program
4.	Implementation of doubly linked list and its operations using C program
5.	Implement different types of inheritance using C++ program
6.	Implementation of C++ program for File streams, File Handling and file operations
7.	Design stack and queue classes with necessary exception handling using Python
8.	Program to implement different types of inheritance using Python
9.	Program to demonstrate the usage of exception handling using Python
10.	Demonstrate Data Visualization using Pandas and Matplotlib packages of Python

Total: 30

REFERENCES/MANUAL/SOFTWARE:

1.	C/C++ interpreter
2.	Python 3 interpreter for Windows/Linux

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	write, test and debug simple programs using control structures and functions in C/C++	Applying(K3), Precision(S3)
CO2	develop real time applications using Object Oriented Programming concepts and database programming	Applying (K3), Precision (S3)
CO3	demonstrate data manipulation and data visualization using Numpy, Pandas and Matplotlib	Applying (K3), Precision(S3)

Mapping of COs with POs						
COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	2		3	3	2	
CO2	3	3	3	3	2	
CO3	1	2	3	3	1	

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

20EST21 EMBEDDED NETWORKING AND BUSES

Programme & Branch	M.E-Embedded Systems	Sem.	Category	L	T	P	Credit
Prerequisites	NIL	**2**	**PC**	**3**	**0**	**0**	**3**

Preamble	To understand the concepts and principles of various buses and networks for embedded applications with respect ISO/OSI standards.	
Unit - I	**Embedded Communication:**	**9**
Modern Instrumentation and Control Systems- Introduction to Networks-Advantages and Disadvantages. OSI Model-Foundations of OSI Model. Protocol – Standards. Grounding, Shielding & Noise		
Unit - II	**Embedded Networking:**	**9**
Introduction – Serial/Parallel Communication – Serial communication protocols: -RS232 standard – RS485 – Synchronous Serial Protocols -Serial Peripheral Interface (SPI)– Inter Integrated Circuits (I2C)– PC Parallel port programming -ISA/PCI Bus protocols		
Unit - III	**USB Protocol** :	**9**
Firewire USB bus – Introduction – Speed Identification on the bus – USB States – USB bus communication: Packets –Data flow types –Enumeration –Descriptors		
Unit - IV	**Industrial Ethernet** :	**9**
Introduction-IEEE Standards-Ethernet MAC layer-IEEE 802.2 and Ethernet SNAP- OSI and IEEE 802.3 standard. Ethernet transceivers, Ethernet types, switches & switching hubs, 10 Mbps Ethernet, 100 Mbps Ethernet, Gigabit Ethernet. TCP / IP Overview- Internet Layer Protocols-Host-to-Host layer		
Unit - V	**Devicenet** :	**9**
Overview – Layers Profibus-Overview-Protocol Stack. HART Protocol – Overview- Layers. Foundation Field Bus- Layers-Error Detection and Diagnostics. CAN Bus – Introduction - Frames –Bit stuffing –Types of errors –Nominal Bit Timing –PIC18Fxx microcontroller CAN Interface		

Lecture:45, Total:45

REFERENCES:

1	Steve Mackay. Edwin Wright, Deon Reynders, John Park, Practical Industrial data Networks: Design, Installation and Trouble Shooting, 1st Edition, Newnes publications-Elsevier 2004.
2	Dogan Ibrahim. Advanced PIC microcontroller projects in C, 1st Edition Newnes publications-Elsevier 2008.
3	Jan Axelson. Parallel Port Complete, 1st Edition, Penram Publications 2000.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	realize the embedded communication with respect OSI model and its standards.	Understanding(K2)
CO2	describe the concepts of Digital Modulation techniques and examine the requirement of Digital communication in today's digital world.	Understanding(K2)
CO3	differentiate Serial communication and Parallel communication	Understanding(K2)
CO4	develop a system to transfer data between peripheral device and microcontroller through USB Protocol	Creating(K5)
CO5	analyze the different IEEE Standards, challenges and its solutions in wireless networks.	Analyzing(K4)

Mapping of COs with POs						
COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1			3	2		
CO2			3	2		
CO3			3	2		
CO4	2		3	2		
CO5	1		3	2		3
1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy						

ASSESSMENT PATTERN - THEORY							
Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	30	70					100
CAT2	30	70					100
CAT3	20	30	10	30	10		100
ESE	10	30	30	15	15		100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

20EST22 RTOS FOR EMBEDDED SYSTEM

Programme & Branch	M.E-Embedded Systems	Sem.	Category	L	T	P	Credit
Prerequisites	NIL	2	PC	3	1	0	4

Preamble	To provide a clear description of the concepts that underlie operating systems such as the ability to complete performance measurements at run-time , to direct the signal or send messages to tasks and to achieve pending on multiple kernel objects.	
Unit - I	**Introduction to Operating Systems:**	**9+3**
Function of OS –Computer system organization – Computer System Architecture - Operating system Operations – Process management – Memory Management – Protection and Security - **System Structures:** Operating system Services – User and Operating system Interface – System calls – Types of System Calls – Operating systems design and Implementation – Operating system Structure.		
Unit - II	**Real Time Systems :**	**9+3**
Overview-System Characteristics-Features of Real time kernels-Implementing real time operating systems - RTOS Concepts: Foreground/Background systems – Real time kernels – RTOS – Scheduling: Preemptive scheduling – Scheduling Points - Round robin scheduling – scheduling Internals		
Unit - III	**µC/OS-III:**	**9+3**
Introduction - µC/OS-III Features - Goals of µC/OS-III – Directories and Files – Critical Sections- Tasks –Task States – Task Scheduling – Idle Task – Statistics Task – Interrupts Under µC/OS-III – Clock Tick - µC/OS-III Initialization. Task Management: Assigning Task Priorities-Determining the size of stack-Detecting Task stack overflows-Task management services-Task Management Internals-Internal Tasks - Time Management.		
Unit - IV	**Resource Management:**	**9+3**
Disable/Enable Interrupts - Lock/Unlock- Semaphores- Mutex semaphore – Deadlock – Synchronization: Semaphore – Task Semaphore – Event Flags -Synchronizing multiple tasks. **Message Passing:** Messages – Messages Queues – Task Message Queue – bilateral rendezvous – Flow control – using message queues – clients and servers – message queue Internals.		
Unit - V	**Memory Management:**	**9+3**
Creating a memory Partition- getting a Memory Block from partition– Returning a Memory Block to a partition-using memory partitions- Porting µC/OS-III: µC/CPU-µC/OS-III Port- Board support Package - Case study of coding for an Automatic Chocolate Vending Machine using MUCOS RTOS.		

Lecture:45, Tutorial:15, Total:60

REFERENCES:

1	A. Silberschatz, P. B. Galvin, G. Gagne, “Operating System Concepts”, 8th Edition, Wiley, 2009.
2	Jean J. Labrosse. µC/OS - III The Real Time Kernel User’s Manual , Micrium Press,.2009.
3	Raj Kamal, "Embedded Systems : Architecture, Programming and Design", 2nd Edition, Tata Mcgraw Hill Education, 2011.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	define the characteristics of real time systems	Remembering(K1)
CO2	realize the concepts of scheduling employed in RTOS	Understanding(K2)
CO3	apply task creation, priority assignment, and time management services provided by µC/OS – III	Applying(K3)
CO4	apply semaphore, mutex, and message queue services in a task	Applying(K3)
CO5	demonstrate memory partitions and allocations techniques used in RTOS and identify the functions involved in porting µC/OS - III to a different architecture	Applying(K3)

Mapping of COs with POs						
COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1			3	2		
CO2			3	2		
CO3	2	2	3	2	2	
CO4	2	2	3	2	2	
CO5	2		3	2		3
1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy						

ASSESSMENT PATTERN - THEORY							
Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	40	60					100
CAT2	10	40	50				100
CAT3		40	60				100
ESE	20	30	50				100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

20EST23 DESIGN OF EMBEDDED SYSTEMS

Programme & Branch	M.E.- Embedded Systems	Sem.	Category	L	T	P	Credit
Prerequisites	NIL	2	PC	3	0	0	3

Preamble	To understand the design and use of single-purpose processors, general-purpose processors and to describe memories and buses.	
Unit - I	**Embedded Design Life Cycle** :	**9**
Embedded Design life cycle – Product specification – Hardware / Software partitioning –Detailed hardware and software design – Integration – Product testing Selection Processes – Microprocessor Vs Micro Controller – Performance tools – Bench marking – RTOS availability – Tool chain availability – Other issues in selection processes.		
Unit - II	**Partitioning Decision:**	**9**
Hardware / Software duality – Coding Hardware – ASIC revolution - Managing the Risk – Co-verification – Execution environment – Memory organization –System startup – Hardware manipulation – Memory mapped access –Speed and code density.		
Unit - III	**Emulator:**	**9**
Interrupt Service routines – Watch dog timers – Flash memory Basic toolset – Host Based debugging – Remote debugging – ROM emulators – logic Analyzer – Caches – Computer optimization – Statistical profiling.		
Unit - IV	**In-Circuit Emulators:**	**9**
Bullet proof run control – Real time trace – Hardware break points – Overlay memory – Timing constraints – Usage issues – Triggers.		
Unit - V	**Testing:**	**9**
Bug tracking – reduction of risks & costs – Performance – Unit testing – Regression testing – Choosing test cases – Functional tests – Coverage tests – Testing embedded software – Performance testing – Maintenance		

Lecture: 45, Total: 45

REFERENCES:

1.	Arnold S. Berger. Embedded System Design, 1st Edition, Taylor& Francis Group, USA 2017.
2.	SriramIyer. Embedded Real time System Programming, Tata McGraw-Hill, India, 2017.
3	Ronald C Arkin. Behaviour-based Robotics, The MIT Press, 2000.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	realize the design flow of an embedded system	Understanding(K2)
CO2	comprehend partitioning decision involved in embedded system design	Understanding(K2)
CO3	Utilize basic tool set used for debugging software and hardware	Applying (K3)
CO4	analyze various in- circuit tool sets for debugging embedded hardware and memories	Applying(K3)
CO5	apply different testing methods involved in test phase for the design of embedded system	Applying(K3)

Mapping of COs with POs						
COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	2		3	2	2	
CO2			2	3	1	
CO3	2		2	3		
CO4	2		2	3		2
CO5	2		2	3		3
1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy						

ASSESSMENT PATTERN - THEORY							
Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	50	50					100
CAT2	20	50	30				100
CAT3	20	50	30				100
ESE	20	40	30				100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

20EST24 EMBEDDED LINUX

Programme & Branch	M.E.- Embedded Systems	Sem.	Category	L	T	P	Credit
Prerequisites	NIL	2	PC	2	0	2	3

Preamble	To develop the embedded RTOS for any target board and to port the RTOS with necessary file system to the target board along with the bootloader.	
Unit - I	**Fundamentals of Linux** :	**6**
Basic Linux System Concepts: Working with Files and Directories - Introduction to Linux File system - Basic Linux commands and concepts Logging in - Shells - Basic text editing - Advanced shells and shell scripting - Processes and threads in Linux - Inter process communication -Linux System calls.		
Unit - II	**Various Distributions And Cross Platform Tool Chain** :	**6**
Introduction - History of Embedded Linux - Embedded Linux versus Desktop Linux - Embedded Linux Distributions - Architecture of Embedded Linux - Linux kernel architecture - User space Linux startup sequence - GNU cross platform Tool chain		
Unit - III	**Host-Target Setup And Overall Architecture:**	**6**
Real Life Embedded Linux Systems -Design and Implementation Methodology - Types of Host/Target Development Setups - Generic Architecture of an Embedded Linux System - System Startup - Types of Boot Configurations System Memory		
Unit - IV	**Kernel Configuration And Root File System** :	**6**
Selecting a Kernel - Configuring the Kernel - Compiling the Kernel - Installing the Kernel - Basic Root File system Structure - Libraries - Kernel Modules and Kernel Images -Setting Up the Bootloader U-boot		
Unit - V	**Embedded Storage And Driver** :	**6**
Memory Technology Device (MTD) MTD Architecture - MTD Driver for NOR Flash The Flash Mapping drivers MTD Block and character devices mtdutils package Embedded File Systems Optimizing storage space-Porting Roadmap Linux serial driver and Ethernet driver		
List of Exercises / Experiments :		
1	Linux file access and shell scripting	
2	Installation of Embedded linux distribution and tool chain for the specified target board	
3	Target Development setup and Boot Configurations	
4	Compiling a kernel, Building a kernel, Configuring kernel modules ,Images for specified target Board	
5	Loading the images in Flash memory	

Lecture:30, Practical:30, Total:60

REFERENCES:

1	Karim Yaghmour. Building Embedded Linux Systems, 2nd Edition, O'Reilly Publications, 2008
2	P.Raghavan ,Amol Lad, Sriram Neelakandan. Embedded Linux System Design and Development, Auerbach Publications, New York, 2006.
3	Paul Cobbaut. Linux Fundamentals, GNU Free Documentation License 2013

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	list the fundamentals of linux OS	Understanding(K2)
CO2	demonstrate Communication between kernel space and user space	Applying(K3)
CO3	develop kernel images for embedded hardware	Applying(K3)
CO4	develop system configuration and boot process	Applying(K3)
CO5	develop the bootloader and configuring the environmental variables for boot process	Applying(K3)
CO6	choose between different software tools for the development of an embedded Linux system	Applying (K3) / Precision(S3)
CO7	develop, report and present design, implementation and application of open source embedded linux	Creating(K6)/ Precision(S3)
CO8	load the developed kernel images to the target board either in RAM or in Flash memory for booting the kernel	Applying(K3)/ Precision(S3)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1				
CO2	3	2	1	1		
CO3	3	2	1	1		
CO4	3	2	1	1		
CO5	3	2	1	1		
CO6	3	2	1	1		
CO7	3	3	3	3	3	
CO8	3	2	1	1		

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1	30	30	30	10			100
CAT2	10	30	40	20			100
CAT3	10	30	40	20			100
ESE	10	40	30	20			100

*** ±3% may be varied * ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

20ESL21 EMBEDDED NETWORKING AND BUSES LABORATORY

Programme & Branch	M.E.- Embedded Systems	Sem.	Category	L	T	P	Credit
Prerequisites	NIL	2	PC	0	0	2	1
Preamble	To impart the knowledge of design and development of embedded products using Microcontroller						

List of Exercises / Experiments :

1.	ISO-OSI Model using Simulation Tools.
2.	Basics of Digital Modulation techniques(Simulation)
3.	Serial port programming RS232 (Simulation/Hardware).
4.	Subnetting using IPV4
5.	TCP and UDP simulation using Netsim
6.	Design and analysis of network using Network simulation Tools
7.	TCP / IP (Simulation/Hardware)
8.	Simulation and analysis of Ethernet
9.	Bit stuffing and character stuffing.
10.	Packet Analysis using Wireshark/Tcpdump

Total: 30

REFERENCES/MANUAL/SOFTWARE:

1.	Netsim
2.	Proteus

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	comprehend the concepts of OSI layer network programming , Basic digital Modulation Techniques and analyze wireless networking concepts of OSI reference model and TCP/IP reference model	Applying(K3), Precision(S3)
CO2	develop a system to transfer data between peripheral device and microcontroller through USB Protocol	Applying (K3), Precision (S3)
CO3	demonstrate a comprehensive theoretical and practical knowledge of the key elements and principles of operation of commonly used automotive networks including: Profibus, HART and CAN bus.	Applying (K3), Precision(S3)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1		2	3	3	2	
CO2	1	3	3	3	2	
CO3		3	3	3	2	

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

20ESP21 - INNOVATIVE PROJECT

Programme & Branch	M.E.- Embedded Systems	Sem.	Category	L	T	P	Credit
Prerequisites	NIL	2	EC	0	0	4	2

Total : 60

COURSE OUTCOMES: On completion of the course, the students will be able to		BT Mapped (Highest Level)
CO1	identify the problem and formulate a problem statement	Applying (K3)
CO2	summarize the literature review	Understanding (K2)
CO3	develop a suitable methodology	Applying (K3)
CO4	carry out the simulation / experimental work as per the specified methodology in embedded domain	Applying (K3)
CO5	prepare and present the project report	Applying (K3)

Mapping of COs with POs and PSOs						
COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	3	3	3	2
CO2	2	3	2	2	2	2
CO3	3	2	3	3	3	3
CO4	3	2	3	3	3	3
CO5	2	3	2	2	3	3
1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy						

20ESP31 - INTERNSHIP CUM PROJECT WORK

Programme & Branch	M.E.- Embedded Systems	Sem.	Category	L	T	P	Credit
Prerequisites	NIL	3	EC	0	0	18	9

Total: 270

COURSE OUTCOMES: On completion of the course, the students will be able to		BT Mapped (Highest Level)
CO1	Formulate a problem statement for the problem given by the industry.	Applying (K3)
CO2	summarize the literature review	Understanding (K2)
CO3	develop a suitable methodology	Applying (K3
CO4	carry out the experimental work and analyse the performance as per the specified methodology in embedded system.	Analyzing (K4)
CO5	prepare and present the project report	Applying (K3)

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	2	3	3	2	3
CO2	2	3	2	2	2	3
CO3	3	2	3	3	3	3
CO4	3	3	3	3	3	3
CO5	2	3	2	2	3	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

20ESP41 - PROJECT WORK

Programme & Branch	M.E.- Embedded Systems	Sem.	Category	L	T	P	Credit
Prerequisites	NIL	4	EC	0	0	18	9

Total : 270

COURSE OUTCOMES: On completion of the course, the students will be able to		BT Mapped (Highest Level)
CO1	identify the problem and formulate a problem statement	Applying (K3)
CO2	summarize the literature review	Understanding (K2)
CO3	develop a suitable innovative methodology	Applying (K3
CO4	carry out the experimental work and analyse the performance as per the specified innovative methodology in embedded system.	Analyzing (K4)
CO5	prepare and present the project report	Applying (K3)

Mapping of COs with POs and PSOs						
COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	2	3	3	2	3
CO2	2	3	2	2	2	3
CO3	3	2	3	3	3	3
CO4	3	3	3	3	3	3
CO5	2	3	2	2	3	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

20ESE01 DISTRIBUTED EMBEDDED COMPUTING

Programme & Branch	M.E.- Embedded Systems	Sem.	Category	L	T	P	Credit
Prerequisites	NIL	1	PE	3	0	0	3

Preamble	This course enables the students to understand the concept of distributed computing infrastructure, concept of Internet and programing language used.	
Unit - I	**The Hardware Infrastructure:**	**9**
Broadband Transmission facilities – Open Interconnection standards – Local Area Networks – Wide Area Networks – Network management – Network Security – Cluster computers.		
Unit - II	**The Internet Concepts:**	**9**
Capabilities and limitations of the Internet – Interfacing Internet server applications to corporate databases HTML and XML Web page design and the use of active components.		
Unit - III	**Distributed Computing using JAVA:**	**9**
IO streaming – Object serialization – Networking – Threading – RMI – multicasting – distributed databases – embedded java concepts – case studies.		
Unit - IV	**Embedded Agent:**	**9**
Introduction to the embedded agents – Embedded agent design criteria – Behaviour based, Functionality based embedded agents – Agent co-ordination mechanisms and benchmarks embedded-agent. Case study: Mobile robots.		
Unit - V	**Embedded Computing Architecture:**	**9**
Synthesis of the information technologies of distributed embedded systems – analog/digital codesign – optimizing functional distribution in complex system design – validation and fast prototyping of multiprocessor system-on-chip – a new dynamic scheduling algorithm for real-time multiprocessor systems.		

Lecture:45,Total:45

REFERENCES:

1	Bernd KleinjohannClab, Architecture and Design of Distributed Embedded Systems, 1st Edition, Kluwer Academic Publisher, Boston, April 2001.
2	George Coulouris and Jean Dollimore, Distributed Systems – concepts and design,5thEdition, Addison – Wesley 2012.
3	SapeMullender, Distributed Systems, 2nd Edition,Addison-Wesley, 1993.
4.	Dietel&Dietel, “JAVA how to program”, 9th Edition,Pearson, 2011.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	understand about the Hardware Infrastructure	Understanding(K2)
CO2	know the concept of Internet for computing applications	Applying(K3)
CO3	use the concept of JAVA in Distributed Embedded Computing	Applying(K3)
CO4	determine the role of embedded agent for simple applications	Applying(K3)
CO5	know the usage of embedded computing architectures	Understanding(K2)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	3	3		
CO2	3		2	2		
CO3	3	2	3	2		
CO4	3	1	2	2		
CO5	3	1	2	2		

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1	**20**	**50**	**30**				**100**
CAT2	**20**	**50**	**30**				**100**
CAT3	**20**	**50**	**30**				**100**
ESE	**30**	**40**	**30**				**100**

*** ±3% may be varied * (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

20ESE02 SOLAR AND ENERGY STORAGE SYSTEM

Programme & Branch	M.E.- Embedded Systems	Sem.	Category	L	T	P	Credit
Prerequisites	NIL	1	PE	3	0	0	3

Preamble	To understand and apply the process of PV systems, power point tracking and design of PV systems.	
Unit - I	**Introduction:**	**9**
Characteristics of sunlight – semiconductors and P-N junctions –behavior of solar cells – cell properties – PV cell interconnection		
Unit - II	**Stand Alone PV System:**	**9**
Schematics, Components, Batteries, Charge Conditioners-Balance of system components for DC and/or AC Applications-Typical applications for lighting, water pumping etc.		
Unit - III	**Grid Connected PV Systems:**	**9**
Schematics, Components, Charge Conditioners, Interface Components-Balance of system Components -PV System in Buildings.		
Unit - IV	**Maximum Power Point Tracking:**	**9**
MPPT concept, Input impedance of DC-DC converters -Boost converter, Buck converter, Buck-Boost converter, PV module in SPICE , Simulation - PV and DC-DC interface-MPPT ALGORITHMS-Impedance control methods, Reference cell, Sampling method, Power slope methods, Hill climbing method, Practical points - Housekeeping power supply, Gate driver, MPPT for non-resistive loads, Simulation.		
Unit - V	**Design of PV Systems:**	**9**
Radiation and load data-Design of System Components for different PV Applications-Sizing and Reliability-Simple Case Studies:Solar Lighting-Solar Cooking-Solar Drying-Solar Desalination-Solar Furnaces.		

Lecture: 45, Total: 45

REFERENCES:

1.	Nayak J.K, Sukhatme S. P. , Solar Energy, 4th Edition,Tata McGraw Hill, 2018.
2.	CHETAN SINGH SOLANKI, Solar Photovotaics–Fundamentals, Technologies and Applications, 3rd Edition, PHI Learning Pvt. Ltd., 2015.
3.	Chenming, Hu. And Richard M.White, Solar Cells from Basic to Advanced Systems, McGraw Hill Book Co, 1983.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	infer the characteristics of sunlight and the role of semiconductors in solar cell	Understanding(K2)
CO2	relate types and design of various PV - interconnected systems.	Applying(K3)
CO3	apply the concepts of MPPT algorithm for PV module in Matlab	Applying(K3)
CO4	choose system components for different PV Applications	Applying(K3)
CO5	infer on Simple case study Solar Lighting-Solar Cooking-Solar Drying-Solar Desalination-Solar Furnaces	Understanding(K2)

Mapping of COs with POs						
COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1			3	2		
CO2			3	2		
CO3	2		3	2		
CO4	1		3	2		
CO5	3		2	3		2
1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy						

ASSESSMENT PATTERN - THEORY							
Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	20	80					100
CAT2	10	50	40				100
CAT3	10	55	35				100
ESE	15	50	35				100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

20ESE03 SEMICONDUCTOR MEMORY DESIGN

Programme & Branch	M.E.- Embedded Systems	Sem.	Category	L	T	P	Credit
Prerequisites	NIL	1	PE	3	0	0	3

Preamble	To study the architectures for SRAM and DRAM, various non-volatile memories, fault modeling and testing of memories for fault detection and the radiation hardening process and issues for memory.	
Unit - I	**Random Access Memory Technologies:**	**9**
SRAM Cell Structures-MOS SRAM Architecture-MOS SRAM Cell and Peripheral Circuit Operation- Bipolar SRAM Technologies-Silicon On Insulator (SOI) Technology- Advanced SRAM Architectures and Technologies-Application Specific SRAMs DRAM Technology Development- CMOS DRAMs- DRAMs Cell Theory and Advanced Cell Structures- BiCMOS, DRAMs- Soft Error Failures in DRAMs- Advanced DRAM Designs and Architecture- Application Specific DRAMs.		
Unit - II	**Nonvolatile Memories :**	**9**
Masked Read-Only Memories (ROMs)- High Density ROMs- Programmable Read-Only Memories (PROMs)- Bipolar PROMs-CMOS PROMs- Erasable(UV) Programmable Road-Only Memories (EPROMs)- Floating-Gate PROM Cell- One-Time Programmable (OTP) EPROMS- Electrically Erasable PROMs (EEPROMs)- EEPROM Technology and Architecture- Nonvolatile SRAM- Flash Memories (EPROMs or EEPROM)- Advanced Flash Memory Architecture.		
Unit - III	**Memory Fault Modeling And Testing:**	**9**
RAM Fault Modeling, Electrical Testing, Peusdo Random Testing- Megabit DRAM Testing- Nonvolatile Memory Modeling and Testing- IDDQ Fault Modeling and Testing- Application Specific Memory Testing.		
Unit - IV	**Semiconductor Memory Reliability:**	**9**
General Reliability Issues- RAM Failure Modes and Mechanism- Nonvolatile Memory Reliability- Reliability Modeling and Failure Rate Prediction- Design for Reliability- Reliability Test Structures- Reliability Screening and Qualification.		
Unit - V	**Packaging Technologies:**	**9**
Radiation Effects- Single Event Phenomenon (SEP)- Radiation Hardening Techniques- Radiation Hardening Process and Design Issues- Radiation Hardened Memory Characteristics-Radiation Hardness Assurance and Testing - Radiation Dosimetry-Water Level Radiation Testing and Test Structures. Ferroelectric Random Access Memories (FRAMs)- Gallium Arsenide (GaAs) FRAMs-Analog Memories- Magnetoresistive Random Access Memories (MRAMs)- Experimental Memory Devices. Memory Hybrids and MCMs (2D)-Memory Stacks and MCMs (3D)-Memory MCM Testing and Reliability Issues-Memory Cards- High Density Memory Packaging Future Directions.		

Lecture:45, Total: 45

REFERENCES:

1. Ashok K. Sharma. Semiconductor Memories: Technology, Testing, and Reliability. 1st Edition, Wiley-IEEE Press, New York. 2002.
2. Ashok K. Sharma. Advanced Semiconductor Memories: Architectures, Designs, and Applications, 1st Edition, Wiley-IEEE Press, New York. 2009.
3. Santhosh K. Kurinec, Krzysztof Iniewski, Nanoscale Semiconductor Memories: Technology and Applications (Devices, Circuits and Systems). 1st Edition. CRC Press, 2017.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	comprehend the micro level operations of Random Access Memories	Understanding(K2)
CO2	analyze the need of non-volatile memories and their applications	Analyzing(K4)
CO3	design the fault free memory systems by fault modeling techniques	Evaluating(K5)
CO4	analyze and design the memory architectures by considering the radiation affects	Analyzing(K4)
CO5	choose packages for memories	Understanding(K2)

Mapping of COs with POs						
COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1			3			
CO2			2	3		
CO3			2	3		
CO4			3	2		
CO5	2		3			
1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy						

ASSESSMENT PATTERN - THEORY							
Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	25	75					100
CAT2	20	50	30				100
CAT3	20	40	25	10	5		100
ESE	20	40	25	10	5		100

*** ±3% may be varied * (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

20ESE04 QT CROSS COMPILING APPLICATION DEVELOPMENT

Programme & Branch	M.E.- Embedded Systems	Sem.	Category	L	T	P	Credit
Prerequisites	Design of Embedded Systems	2	PE	3	0	0	3

Preamble	To know the basic concepts of Qt - single cross platform and to use C++ tool to design, develop, test, deploy programs for projects.	
Unit - I	**Introduction to C++**	**9**
Basic Concepts - Conditionals and Loops - Data Types, Arrays, Pointers – Functions -Classes and Objects - Inheritance & Polymorphism – sample programs.		
Unit - II	**QT installation and compilation**	**9**
Qt Basics – features - Qt Widgets - Learning the landscape – Build pro file - breakpoints – Examining variables and memory - Projects pane and building project - Example with Qt Widgets.		
Unit - III	**Qt Designer**	**9**
Main form - application resources - Instantiating forms - message boxes - dialogs - Wiring the Qt Widgets application logic - declarative user interface development.		
Unit - IV	**Qt IoT**	**9**
Representing data using core classes - key-value pairs – Multithreading - Accessing files - Accessing HTTP resources - XML parsing with HTTP.		
Unit - V	**Application development**	**9**
Managing widget layout – Model View Controller programming - Analyzing a concrete model subclass - MVC model on Qt Creator – sample applications development.		

Lecture:45, Total: 45

REFERENCES:

1. Lee ZhiEng, Ray Rischpater, Application Development with Qt Creator, 3rd Edition, Packt Publishing Ltd, Birmingham, UK, 2020.
2. Herbert Schildt, C++: The Complete Reference , 4th Edition, Osborne McGraw-Hill, U.S.A. 2017.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	use class level C++ programs for simple applications.	Applying(K3)
CO2	apply programming concepts for simple application.	Applying(K3)
CO3	develop graphic user interface.	Applying(K3)
CO4	apply Qt for Internet of things.	Applying(K3)
CO5	develop basic applications for different OS platform.	Applying(K3)

Mapping of COs with POs						
COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1			3	2		
CO2			3	2		
CO3	2		3	2		1
CO4			3	1		
CO5	2		3	3	2	2
1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy						

ASSESSMENT PATTERN - THEORY							
Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	10	30	60				100
CAT2	10	30	60				100
CAT3	10	30	60				100
ESE	10	30	60				100

*** ±3% may be varied * (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

20ESE05 SENSORS AND ACTUATORS FOR ROBOTICS

Programme & Branch	M.E.- Embedded Systems	Sem.	Category	L	T	P	Credit
Prerequisites	NIL	2	PE	3	0	0	3

Preamble	To learn and analyze the parameters components of robotics such as parallel and grippers , manipulators, sensors and actuators	
Unit - I	**Introduction :**	**9**
Definition and origin of robotics – different types of robotics – various generations of robots – degrees of freedom – Asimovs laws of robotics – dynamic stabilization of robots.		
Unit - II	**Sensors and Actuators:**	**9**
Sensors: Machine vision – ranging – laser – acoustic– magnetic, fiber optic and tactile sensors. Actuators: Manipulator dynamics and force control – electronic and pneumatic manipulator control circuits – end effectors – various types of grippers – design considerations. Drives: Hydraulic, pneumatic and electric drives		
Unit - III	**Mechatronics:**	**9**
Determination of HP of motor and gearing ratio – variable speed arrangements – path determination Solution of inverse kinematics problem – multiple solution jacobian work envelop – hill Climbing Techniques.		
Unit - IV	**Robot Programming:**	**9**
Introduction to robot programming languages – classification of robot languages – Computer control and robot software – VAL system and Language		
Unit - V	**Applications of Robots**:	**9**
Mutiple robots – machine interface – robots in manufacturing and non- manufacturing applications – robot cell design – selection of robot.		

Lecture: 45, Total: 45

REFERENCES:

1. Deb. S.R. Robotics Technology and flexible Automation, 2nd Edition, McGraw Hill Publication, New Delhi,2010.
2. Nicholas Odrey, Mitchell Weiss, Mikell Groover, Roger N.Nagel, Ashish Dutta, Industrial Robotics, 2nd Edition, McGraw-Hill Singapore, 2012.
3. Ghosh, Control in Robotics and Automation: Sensor Based Integration, 1st Edition, Allied Publishers, Chennai,1999.
4. Richard D. Klafter, Thomas A. Chmielewski, Michael Negin, Robotic Engineering: An Integrated Approach, 1st Edition , Prentice Hall India, New Delhi, 2007.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	describe the functions of a robot.	Remembering(K1)
CO2	analyze the type of sensors, actuators and drives for robots.	Analyzing(K4)
CO3	apply the kinematics and path planning for robot applications.	Applying(K3)
CO4	experiment robot operations using VAL robot programming language.	Applying(K3)
CO5	develop robots for manufacturing Industries.	Creating(K6)

Mapping of COs with POs						
COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1			3	2		
CO2	1		3	2		
CO3	1		3	2		
CO4			3	2		
CO5	2		2	3	1	2
1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy						

ASSESSMENT PATTERN - THEORY							
Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	30	20	30	20			100
CAT2	10	10	65	15			100
CAT3		20	60	5		15	100
ESE	10	20	50	10		10	100

*** ±3% may be varied * (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

20ESE06 VERILOG HDL FOR EMBEDDED FPGA PROCESSOR

Programme & Branch	M.E.- Embedded Systems	Sem.	Category	L	T	P	Credit
Prerequisites	NIL	2	PE	3	0	0	3

Preamble	To understand the fundamentals of Verilog HDL programming and interfacing techniques for various Embeded FPGA processor.	
Unit - I	**Verilog concepts:**	**9**
Introduction- Design flow- Design hierarchy- components of a simulation- Basic concepts- Data types- System tasks and compiler Directives-Modules and ports-test bench.		
Unit - II	**Modeling with Verilog HDL:**	**9**
Overview of digital design using Verilog-HDL--Gate level Modeling-Dataflow Modeling-Behaviour Modeling-Tasks and Functions-Switch level modeling.		
Unit - III	**Logic Synthesis with Verilog HDL:**	**9**
Verilog HDL Synthesis-Synthesis Design Flow-Verification of the gate level net list Modeling for logic synthesis-Example of sequential circuit synthesis.		
Unit - IV	**Digital System Design:**	**9**
Design of a FSM: Mealy and Moore outputs, FSM representation, FSM code development and Design examples. Design of FSMD: Single RT operation, ASMD chart, Code development of an FSMD, Design examples.		
Unit - V	**Embedded FPGA Processor and Interfacing**	**9**
Overview of FPGA Device and EDA software- FPGA, Xilinx Spartan3 devices, Digilent S3 board, Development flow and Xilinx ISE Project Navigator. UART interface, Seven Segment Interface, Keyboard/Mouse Interface.		

Lecture: 45, Total: 45

REFERENCES:

1.	Samir Palnitkar, Verilog HDL: A Guide to Digital Design and Synthesis, 2nd Edition, Pearson Education, New Delhi, 2003.
2.	Pong P. Chu, FPGA Prototyping By Verilog Examples Xilinx Spartan-3 Version, A John Wiley & Sons, INC, Publication, New Jersey, 2008.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	recall the Verilog programming concepts about data types, modules and test bench.	Remembering(K1)
CO2	comprehend the gate level, data flow, behavioral and switch level modeling techniques of Verilog programming	Understanding(K2)
CO3	design and synthesize combinational and sequential circuits using Verilog programming	Applying(K3)
CO4	design finite state machine circuits using Verilog programming	Applying(K3)
CO5	examine the interface peripherals with embedded Xilinx Spartan 3 FPGA processor	Understanding(K2)

Mapping of COs with POs						
COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	3		2	2		
CO2	2		3	2	3	
CO3	1		3	3	3	
CO4	1		3	3	2	
CO5	2		1	2	2	
1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy						

ASSESSMENT PATTERN - THEORY							
Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	40	60					100
CAT2	20	40	40				100
CAT3	10	30	60				100
ESE	20	40	40				100

*** ±3% may be varied * (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

20ESE07 COMPUTER BASED INDUSTRIAL CONTROL

Programme & Branch	M.E.- Embedded Systems	Sem.	Category	L	T	P	Credit
Prerequisites	NIL	2	PE	3	0	0	3

Preamble	To know the need, levels different technologies in robotics and programming aspects of PLC for real time applications in industrial automation.	
Unit - I	**Introduction:**	**9**
Automation in Production System, Principles and Strategies of Automation Basic Elements of an Automated System, Advanced Automation Functions, Levels of Automations.		
Unit - II	**Control Technologies in Automation:**	**9**
Industrial Control Systems, Process Industries Versus Discrete-Manufacturing Industries, Continuous Versus Discrete Control, sensors and actuators and other control system components.		
Unit - III	**Robotics in industrial Automation:**	**9**
Robot anatomy and Related Attributes, Robot control systems, End Effectors, Sensors in Robotics, Industrial Robot Applications ,Robot programming, Engineering analysis of Robots**.**		
Unit - IV	**PLC in industrial Automation:**	**9**
Introduction to PLC, Discrete Process Control: logic control- sequencing, ladder logic diagrams, Programmable logic controllers: components of the PLC-PLC operating cycle-additional capabilities of the PLC- Programming the PLC, Personal computers using soft logic.		
Unit - V	**Case Studies and Safety measures:**	**9**
Industrial Control Applications: Cement, Thermal, Water Treatment, Steel Plants, Process Control plant, Textile & Dyeing industries, Industrial safety measures.		

Lecture: 45, Total: 45

REFERENCES:

1.	Mikell P.Groover Automation, Production Systems and Computer Integrated Manufacturing, 5th Edition, Pearson Education., 2018.
2.	Krishna Kant, Computer Based Industrial Control, 2nd Edition, PHI Learning Pvt. Ltd.,2010.
3	W. Bolton, Programmable Logic Controllers", 6th Edition, Jonathan Simpson ,USA, 2015.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	identify the principles, elements and levels of integrated industrial automation system.	Understanding(K2)
CO2	realize industrial control systems and analyze of continuous and discrete technologies with different sensors and actuators.	Understanding(K2)
CO3	point out the anatomy, applications and programming methods of robotics for industrial automation.	Understanding(K2)
CO4	write programming for PLC based industrial application	Applying(K3)
CO5	apply the industrial automation concepts for real-time applications and select the industrial safety measures.	Applying(K3)

Mapping of COs with POs						
COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	2		3	2		
CO2			2	3		
CO3			2	3		
CO4			3	2		
CO5	2		3	3	1	1
1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy						

ASSESSMENT PATTERN - THEORY							
Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	40	60					100
CAT2	25	75					100
CAT3	20	60	20				100
ESE	5	75	20				100

*** ±3% may be varied * (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

20ESE08 RISC PROCESSOR

Programme & Branch	M.E.- Embedded Systems	Sem.	Category	L	T	P	Credit
Prerequisites	NIL	2	PE	3	0	0	3

Preamble	To design the embedded system applications with AVR and ARM microprocessors employing the knowledge of different user peripherals and operating systems.	
Unit - I	**AVR Microcontroller Architecture:**	**9**
Architecture – memory organization – addressing modes – I/O Memory – EEPROM – I/O Ports-SRAM –Timer –UART – Interrupt Structure- Serial Communication with PC – ADC/DAC Interfacing.		
Unit - II	**ARM Architecture And Programming:**	**9**
Arcon RISC Machine -Core & Architectures -- The ARM Programmer's model -Registers – Pipeline - Interrupts - Coprocessors. Instruction set – Thumb instruction set – Instruction cycle timings System Peripherals: Bus structure –Memory map –Memory accelerator module –External bus interface –Phase Locked Loop –VLSI peripheral bus divider –Power control		
Unit - III	**User Peripherals** :	**9**
Pin connect block –General purpose I/O –Timers –Capture –Compare –PWM modules–Watchdog timer –Analog to digital converter-UART –I2C interface –SPI interface –CAN interface		
Unit - IV	**Memory Protection And Management**:	**9**
Protected Regions-Initializing MPU, Cache and Write Buffer-MPU to MMU-Virtual Memory-Page Tables- TLB-Domain and Memory Access Permission-Fast Context Switch Extension.		
Unit - V	**ARM Application Development:**	**9**
Introduction to DSP on ARM – Filter –Exception Handling – Interrupts – Interrupt handling schemes- Firmware and boot loader – Example: Standalone - Embedded Operating Systems – Fundamental Components.		

Lecture: 45, Total: 45

REFERENCES:

1.	Andrew N. Sloss, Dominic Symes, Chris Wright, John Rayfield, ARM System Developer's Guide Designing and Optimizing System Software, 1st Edition,Morgan, Kaufmann/Elsevier, 2009.
2.	Dananjay V. Gadre, Programming and Customizing the AVR microcontroller, 1st Edition McGraw-Hill, 2001.
3	Trevor Martin, The Insider's Guide to the Philips ARM7-Based microcontrollers: An Engineer's Introduction To The LPC2100 Series, Coventry Hitex (UK) Ltd, 2005.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	use timer, UART and ADC modules of Atmega2560 microcontroller for I/O applications	Applying(K3)
CO2	realize the architecture and instruction set of ARM7.	Understanding(K2)
CO3	use configurations of PLL and bus structures in LPC21xx for frequency generations.	Applying(K3)
CO4	design Industrial applications with peripheral interface using LPC21xx.	Applying(K3)
CO5	relate and differentiate MMU, MPU and Virtual Memory concepts.	Applying(K3)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1			3	2		
CO2			3	2		
CO3	1		2	3		
CO4	2		3	2		
CO5			3	2	2	2

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1	20	50	30				100
CAT2	20	50	30				100
CAT3	20	40	40				100
ESE	20	40	40				100

*** ±3% may be varied * (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

20ESE09 DESIGN OF EMBEDDED CONTROL SYSTEM

Programme & Branch	M.E.- Embedded Systems	Sem.	Category	L	T	P	Credit
Prerequisites	Design of Embedded Systems	2	PE	3	0	0	3

Preamble	To introduce the basic concepts of control systems and its embedded implementation.	
Unit - I	**CONTROL SYSTEM BASICS**	**9**
Z-transforms – performance requirements - block diagrams - analysis and design - sampling theory – difference equations.		
Unit - II	**CONTROL SYSTEM IMPLEMENTATION**	**9**
Discretization method – Fixed point mathematics – Nonlinear controller elements – Gain scheduling – Controller implementation and testing in Embedded Systems - a case study of robotic control system.		
Unit - III	**CONTROL SYSTEM TESTING:**	**9**
Software implications - Controller implementation and testing in embedded systems - Measuring frequency response.		
Unit - IV	**INPUT DEVICES:**	**9**
Keyboard basics - Keyboard scanning algorithm - Character LCD modules - LCD module display Configuration - Time-of-day clock - Timer manager - Interrupts - Interrupt service routines - Interrupt-driven pulse width modulation. Triangle waves analog vs. digital values - Auto port detect - Capturing analog information in the timer interrupt service routine - Automatic, multiple channel analog to digital data acquisition.		
Unit - V	**OUTPUT DEVICES AND SENSORS**	**9**
H Bridge – relay drives - DC/ Stepper Motor control – optical devices. Linear and angular displacement sensors: resistance sensor – induction displacement sensor – digital optical displacement sensor – pneumatic sensors. Speed and flow rate sensors: electromagnetic sensors – fluid flow sensor – thermal flow sensor. Force sensors: piezoelectric sensors – strain gauge sensor – magnetic flux sensor – inductive pressure sensor – capacitive pressure sensor. Temperature sensors: electrical – thermal expansion – optical Case Study- Examples for sensor, actuator, control circuits with applications.		

Lecture:45, Total: 45

REFERENCES:

1.	Jim Ledin, Embedded control systems in C/C++, 1st Edition, CMP Books,2004.
2.	TimWiscott, Applied control for embedded systems, 1st Edition, Elsevier Publications, 2006.
3	Jean J. Labrosse, Embedded Systems Building Blocks: Complete and Ready-To-Use Modules in C, 1st Edition, The Publisher, Paul Temme, 2011.
4	Ball S.R., Embedded microprocessor Systems - Real World Design, 3rd Edition, Prentice Hall, 2002.
5	Lewin A.R.W. Edwards, Open source robotics and process control cookbook, 1st Edition, Elsevier Publications, 2005.
6	Ben-Zion Sandler, Robotics, 1st Edition, Elsevier Publications, 1999.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	identify the basics of control systems.	Understanding(K2)
CO2	Implement control theory in embedded systems.	Applying(K3)
CO3	Appraise the concept of control system in testing	Understanding(K2)
CO4	Apply the concept in the applications using control systems	Applying(K3)
CO5	Infer the input and output devices used in control systems.	Understanding(K2)

Mapping of COs with POs						
COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1			3	2		
CO2	1		3	2		
CO3			1	3		
CO4	1		3	2		
CO5			3	2		
1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy						

ASSESSMENT PATTERN - THEORY							
Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	20	40	40				100
CAT2	20	40	40				100
CAT3	20	50	30				100
ESE	20	50	30				100

*** ±3% may be varied * ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks) (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

20ESE10 NATURE INSPIRED OPTIMIZATION TECHNIQUE

Programme & Branch	M.E.- Embedded Systems	Sem.	Category	L	T	P	Credit
Prerequisites	NIL	3	PE	3	0	0	3

Preamble	To acquaint and familiarize with different types of optimization techniques, solving optimization problems, implementing computational techniques, abstracting mathematical results and proofs etc.	
Unit - I	**Introduction to Algorithms:**	**9**
Newton's Method – Optimization - Search for Optimality - No-Free-Lunch Theorems - 1.6 Nature-Inspired Metaheuristics - Brief History of Metaheuristics Analysis of Algorithms : Introduction - Analysis of Optimization Algorithms - Nature-Inspired Algorithms - Parameter Tuning and Parameter Control.		
Unit - II	**Simulated Annealing:**	**9**
Annealing and Boltzmann Distribution - Parameters - SA Algorithm - Unconstrained Optimization - Basic Convergence Properties SA Behavior in Practice - Stochastic Tunneling Genetic Algorithms : Introduction - Genetic Algorithms - Role of Genetic Operators - Choice of Parameters - GA Variants - Schema Theorem - Convergence Analysis.		
Unit - III	**Particle Swarm Optimization:**	**9**
Swarm Intelligence - PSO Algorithm - Accelerated PSO – Implementation - Convergence Analysis - Binary PSO - Problems Cat Swarm Optimization : Natural Process of the Cat Swarm - Optimization Algorithm – Flowchart - Performance of the CSO Algorithm.		
Unit - IV	**TLBO Algorithm, Cuckoo Search & Bat Algorithms**	**9**
TLBO Algorithm :Introduction **-** Mapping a Classroom into the Teaching-Learning-Based optimization – Flowchart- Problems **Cuckoo Search :** Cuckoo Life Style - Details of COA – flowchart - Cuckoos' Initial Residence Locations - Cuckoos' Egg Laying Approach - Cuckoos Immigration - Capabilities of COA **Bat Algorithms** - Echolocation of Bats - Bat Algorithms – Implementation - Binary Bat Algorithms - Variants of the Bat Algorithm - Convergence Analysis		
Unit - V	**Other Algorithms:**	**9**
Ant Algorithms - Bee-Inspired Algorithms - Harmony Search - Hybrid Algorithms		

Lecture: 45, Total: 45

REFERENCES:

1.	Xin-She Yang, Nature-Inspired Optimization Algorithms, 1st Edition, Elsevier, 2014
2.	Omid Bozorg-Haddad , Advanced Optimization by Nature-Inspired Algorithms Studies in Computational Intelligence,1st Edition, Springer Series, 2018
3	Srikanta Patnaik, Xin-She Yang ,Kazumi Nakamatsu, Nature-Inspired Computing and Optimization Theory and Applications, 1st Edition, Springer Series, 2017

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	infer the concepts of optimization techniques	Understanding(K2)
CO2	identify the parameter which is to be optimized for an application	Applying(K3)
CO3	differentiate the concepts of different optimization algorithms and create mathematical optimization models	Applying(K3)
CO4	select suitable optimization algorithm for a real time application	Applying(K3)
CO5	make recommendations based on solutions, analyses, and limitations of models	Applying(K3)

Mapping of COs with POs						
COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	2		3	2		
CO2	1		2	3		
CO3	2		3	2		
CO4	3		2	3		2
CO5	2		2	3		2
1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy						

ASSESSMENT PATTERN - THEORY							
Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	40	40	20				100
CAT2	40	40	20				100
CAT3	20	40	40				100
ESE	30	40	30				100

*** ±3% may be varied * (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

20ESE11 SUPERVISED MACHINE LEARNING ALGORITHMS

Programme & Branch	M.E.- Embedded Systems	Sem.	Category	L	T	P	Credit
Prerequisites	NIL	3	PE	3	0	0	3

Preamble	To focus on supervised machine learning algorithms to create simple, interpretable models to solve classification and regression problem.	
Unit - I	**Discriminative Algorithms :**	**9**
Cost function –LMS Algorithm – The normal Equations-Probability interpretation-locally weighted linear regression-logistic regression-generalized linear models-Application to prediction		
Unit - II	**Generative Algorithms :**	**9**
Generative Models: Gaussian Discriminant Analysis(GDA)-Naïve Bayes- Laplace smoothing-Marginal classifier: Support Vector Machine (SVM) as optimal Margin classifier-Application to Classification.		
Unit - III	**Neural Networks:**	**9**
ANN Architecture- Parameter Initialization -Forward Propagation- Activation Functions (Sigmoid,tanh,relu)-Training and Optimization with back propagation-Learning Boolean Functions		
Unit - IV	**Convolutional Neural Networks (CNN) :**	**9**
Convolution kernel-Pooling (Max Pooling, fractional Pooling)-Strides-Fully Connected Layers –Loss functions – MiniBatch Training - Optimization – Application to MNIST image classification		
Unit - V	**Fine Tuning :**	**9**
Regularization: Bias-Variance-Bias-variance Trade off- Initialization of parameters (Xavier)-Cross Validation-Data Augmentation-dropouts-Batch Normalization.		

Lecture: 45, Total: 45

REFERENCES:

1.	Christopher M. Bishop, Pattern Recognition and Machine Learning, Springer-Science+Business Media, New York. reprint 2010
2.	Trevor Hastie, The Elements of Statistical Learning: Data Mining, Inference, and Prediction, 2nd Edition, , Springer series in Statistics, 2009
3	UCI Machine Learning repository: http://archive.ics.uci.edu/ml/index.php

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	analyse and apply discriminative algorithms for classification and regression problems	Analyzing(K4)
CO2	validate a generative model based algorithm for classification and regression problems	Analyzing(K4)
CO3	analyse the designed ANN for a real time application using BPN	Analyzing(K4)
CO4	develop a CNN model for image analysis.	Applying(K3)
CO5	analyse various metrics used in fine tuning supervised learning models	Analyzing(K4)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3				3	
CO2	1		2		3	
CO3	1		2		3	
CO4	1				3	
CO5	1	3				

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1	6	53	24	16			100
CAT2	6	53	24	16			100
CAT3	6	66	28				100
ESE	4	60	20	16			100

*** ±3% may be varied * (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

20ESE12 SIGNAL AND IMAGE PROCESSING FOR REAL TIME APPLICATIONS

Programme & Branch	M.E.- Embedded Systems	Sem.	Category	L	T	P	Credit
Prerequisites	NIL	3	PE	3	0	0	3

Preamble:	To develop the image processing tools from scratch, rather than using any image processing library functions	
Unit - I	**Digital Image Fundamentals** :	**9**
Elements of digital image processing systems- Brightness- Contrast- Hue- saturation- Mach band effect -2D Image sampling- 2D Image transforms: DCT – KLT – Haar. Image Enhancement: Basic intensity transformations – Histogram equalization - Spatial filtering : Smoothing and sharpening Filters – Frequency domain filtering : Smoothing and sharpening filters – Homomorphic filters		
Unit - II	**Morphological Image Processing :**	**9**
Erosion – Dilation – Duality – Opening – Closing – Hit or Miss Transformation– Basic Morphological Algorithms : Boundary Extraction- Hole filling – Extraction of connected components – Thinning – Thickening – Grayscale Morphology – Morphological smoothing – Morphological gradient – Tophat and bottom hat transformation		
Unit - III	**Image Segmentation** :	**9**
Point, line and edge detection – Basics of intensity thresholding – Region based segmentation: Region growing - Region splitting and merging. Image Compression: Fundamentals: Types of redundancy – Huffmann – Run length coding – Arithmetic coding - Block Transform coding		
Unit - IV	**Pattern recognition** :	**9**
Patterns and Pattern classes – Representation of Pattern classes – Approaches to object recognition :Baye's Parametric classification – Template matching method – Structural Pattern Recognition : statistical and structural approaches		
Unit - V	**Overview of speech processing** :	**9**
Speech Fundamentals: Articulatory Phonetics – Production and Classification of Speech Sounds; Acoustic Phonetics – acoustics of speech production; Short time Homomorphic Filtering of Speech; Linear Prediction (LP) analysis: Basis and development, LPC spectrum.		

Lecture: 45, Total: 45

REFERENCES:

1.	Gonzalez.R.C, Woods.R.E, Digital Image Processing, 4th Edition, Pearson Education, 2009
2.	Jayaraman.S, Esakkirajan.S, Veerakumar.T, Digital Image Processingll, 1st Edition Tata McGraw-Hill, New Delhi, , 2009.
3	Hayes, Monson H. Statistical Digital Signal processing and Modeling, 1st Edition, John Wiley and Sons, Inc., 1996

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	interpret the basic image processing spatial domain characteristics of digital images	Understanding(K2)
CO2	apply Haar, DCT and KL Transforms to transform from spatial domain to other domains	Applying(K3)
CO3	apply morphological operators and segmentation algorithms to extract the edges and regions of interest	Applying(K3)
CO4	employ Huffmann, Arithmetic, Runlength and nblock transform coding techniques and compress the images	Applying(K3)
CO5	Outline the pattern recognition and speech processing approaches	Analyzing(K4)

Mapping of COs with POs						
COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1			3	3		
CO2			3	2		
CO3	2		3	3		
CO4	2		3	3		
CO5			2	3		
1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy						

ASSESSMENT PATTERN - THEORY							
Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	20	40	40				100
CAT2	20	30	50				100
CAT3	20	30	40	10			100
ESE	20	30	40	10			100

*** ±3% may be varied * (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

20ESE13 PROGRAMMING INTERNET OF THINGS

Programme & Branch	M.E.- Embedded Systems	Sem.	Category	L	T	P	Credit
Prerequisites	NIL	4	PE	3	0	0	3

Preamble	To learn the fundamentals of this emerging technology and to design of smart objects that provide collaboration and ubiquitous services.	
Unit - I	**IoT ARCHITECTURE:**	**9**
IoT Architecture-State of the Art – Introduction, State of the art, Reference Model and architecture, IoT reference Model - IoT Reference Architecture Introduction, Functional View, Information View, Deployment and Operational View, Other Relevant architectural views. Real-World Design Constraints- Introduction, Technical Design constraints-hardware is popular again, Data representation and visualization, Interaction and remote control.-IOT Communication Models-Communication API's-IOT Enabling Technologies.		
Unit - II	**IoT LEVELS ,M2M,AND SYSTEM MANAGEMENT**:	**9**
IoT Levels1 to 6—M2M-Difference between IoT and M2M –SDN and NFV-Need of IoT system Management- with NETCONF and YANG, IoT Design Methodology.		
Unit - III	**INTEROPERABILITY IN IoT, INTRODUCTION TO PROGRAMMING PYTHON:**	**9**
Data types – Data structures – Control flow – Functions – Modules – Packages – File Handling – Date and time operation – Classes – Python packages of IoT. IoT Physical Design: Basic building blocks – Raspberry Pi –Linux on Raspberry Pi –GPIO-Interfaces(LED and Switch) – Programming on Raspberry Pi with Python		
Unit - IV	**DATA ANALYTICS AND WEB FRAMEWORK:**	**9**
Data Analytics for IOT: Apache Handoop-Map Reduce Models-Case Study : Batch Data Analysis and Real Time Data Analysis. Web Application Framework: Django,-Django Architecture-starting Development with Django.		
Unit - V	**CASE STUDIES:**	**9**
LAMP Installation– Home temperature monitoring system – Webcam and Raspberry Pi camera project, A Raspberry Pi LASER trip wire, Line follower Robot.		

Lecture: 45, Total: 45

REFERENCES:

1.	Arshdeep Bahga, Vijay K. Madisetti—Internet of Things: A Hands-on Approach, 1stEdition, Universities Press-Hyderabad, 2015.
2.	Donald Norris —The Internet of Things: Do-It-Yourself at Home Projects for Arduino, Raspberry Pi and Beagle Bone Black, 1st Edition, McGraw Hill, 2015
3	Peter Waher — Learning Internet of Things, 1st Edition, Packt Publishing Limited - USA, 2015.
4	https:\\projects. Raspberry Pi.org

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	compare the IoT physical and logical Architecture and its Enabling Technologies	Understanding(K2)
CO2	interpret Different IoT Levels and Networking Methodologies	Understanding(K2)
CO3	implement IoT Programming Concepts using Python and its Open Source Tools	Applying(K3)
CO4	Perform Data Analysis using –Hadoop & ,Django	Applying(K3)
CO5	design and integrate projects using Raspberry Pi with Temperature Sensor, Webcam	Applying(K3)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1			2	3		
CO2			2	3		
CO3	2		3	2		
CO4	2		2	3		
CO5	2	2	3	3	3	2

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1	20	40	40				100
CAT2	20	50	30				100
CAT3	20	50	30				100
ESE	20	50	30				100

*** ±3% may be varied * (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

20ESE14 SINGLE BOARD COMPUTER

Programme & Branch	M.E.- Embedded Systems	Sem.	Category	L	T	P	Credit
Prerequisites	NIL	4	PE	3	0	0	3

Preamble	To develop a basic knowledge in working with single board computer for multifunctional tasks like IoT, Image analysis for research applications.	
Unit - I	**Introduction To SBC and Linux Basics:**	**9**
Types of single board computer **-** Linux file system - text editors - accessing files - power supply unit - preparation of boot SD card - configuration - networking with Host computer - terminal access.		
Unit - II	**Python Programming and Sensor Interfacing:**	**9**
Pin diagram - GPIO access - LED & Switch - Timers - external circuit interfacing - UART - sensor interfacing.		
Unit - III	**Peripheral Control:**	**9**
Interfacing touch screen - ADC, DAC and, Motor - DC Motor Control using PWM Relay and Stepper Motor interfacing.		
Unit - IV	**Internet of Things:**	**9**
Open API's for Internet of Things - collect and store sensor data - analyze and visualize data - control peripheral device.		
Unit - V	**Image Processing in SBC:**	**9**
Introduction to OPENCV - reading and writing images - create image - draw - conversion - merge - video processing - real-time image processing in SBC.		

Lecture: 45, Total: 45

REFERENCES:

1.	Simon Monk. Raspberry Pi Cookbook: Software and Hardware Problems and Solution, 3rd Edition, O'Reilly Media Inc , California, USA, 2020.
2.	Guillermo Guillen. Sensor Projects with Raspberry Pi: Internet of Things and Digital Image Processing, 1st Edition, A Press Media,New York, 2019.
3	Joseph Howse, Joe Minichino. Learning Open CV 4 Computer Vision with Python 3, 3rdEdition, PacktPublishing Ltd., Birmingham, UK, 2020.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	program the ports and peripherals of SBC	Applying(K3)
CO2	write program for real time applications using SBC	Applying(K3)
CO3	describe peripherals using interfacing techniques	Applying(K3)
CO4	choose devices for Internet of things	Understanding(K2)
CO5	apply image processing for real time applications	Applying(K3)

Mapping of COs with POs						
COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1		1	3	2		
CO2	2	2	3	2	2	2
CO3			3	2		
CO4			3	3		
CO5	2		3	2	2	3
1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy						

ASSESSMENT PATTERN - THEORY							
Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	10	30	60				100
CAT2	10	30	60				100
CAT3	10	40	50				100
ESE	10	35	55				100

*** ±3% may be varied * (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

20ESE15 SYSTEM ON CHIP FOR EMBEDDED APPLICATIONS

Programme & Branch	M.E.- Embedded Systems	Sem.	Category	L	T	P	Credit
Prerequisites	Nil	4	PE	3	0	0	3

Preamble	To know the architecture of embedded processor like ARM processor and to study different operating systems	
Unit - I	**Introduction to System on Chip Design:**	**9**
Processor architecture and organization ,Abstraction in hardware design, MU0 - a simple processor, Instruction set design , Processor design trade-offs, The Reduced Instruction Set Computer, Design for low power consumption, ARM architecture.		
Unit - II	**ARM Organization and Implementation:**	**9**
3-stage pipeline ARM organization, 5-stage pipeline ARM organization, ARM instruction execution and implementation, coprocessor interface, The ARM instruction set and programming.		
Unit - III	**ARM Processor Cores and Memory Hierarchy:**	**9**
ARM7TDMI, ARM8, and ARM9TDMI ARM10TDMI - Memory size and speed, On-chip memory, Caches, Cache design - an example,Memory management.		
Unit - IV	**Architectural Support for Operating Systems:**	**9**
An introduction to operating systems, The ARM system control coprocessor,CP15 protection unit registers, ARM protection unit, CP15 MMU registers, ARM MMU architecture, Synchronization, Context switching, Input/output.		
Unit - V	**Embedded ARM Applications:**	**9**
The VLSI Ruby II Advanced Communication Processor, The VLSI ISDN Subscriber Processor, The Ericsson-VLSI Bluetooth Baseband Controller, The ARM7500 and ARM7500FE, case study on The DRACO telecommunications controller		

Lecture: 45, Total: 45

REFERENCES:

1.	Steve Furber. ARM System-on-Chip Architecture, 2nd Impression, Pearson Education, 2009.
2.	Andrew N. Sloss , Dominic Symes, Chris Wright. ARM System Developer's Guide: Designing and Optimizing System Software, 1st Edition, Morgan Kaufmann Publishers **,** 2004.
3	Joseph Yiu. The Definitive Guide to ARM® Cortex®-M3 and Cortex®-M4 Processors, 3rd Edition, Newnes publication, 2014.
4	Yifeng Zhu. Embedded Systems with ARM Cortex-M Microcontrollers in Assembly Language and C, 3rd Edition, E-Man Press LLC, 2017.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	identify the basic design of system on chip with ARM architecture as a reference	Understanding(K2)
CO2	Know the 3-line and 5-line pipelining concept of ARM organisation and programming with instruction set	Understanding(K2)
CO3	realize the memory hierarchy and design of different ARM7, ARM8, ARM9 and ARM10 processor cores	Applying(K3)
CO4	realize the concept of ARM operating systems, ARM protection unit and MMU.	Applying(K3)
CO5	apply the system on chip concept for different embedded applications such as ISDN, Bluetooth and DRACO telecommunication controller	Applying(K3)

Mapping of COs with POs						
COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1			3	2		
CO2			3	2		
CO3	2		3	2		
CO4	2		3	2		
CO5	3		3	2		2
1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy						

ASSESSMENT PATTERN - THEORY							
Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	30	50	20				100
CAT2	30	40	30				100
CAT3	30	40	30				100
ESE	30	40	30				100

*** ±3% may be varied * (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

20ESE16 SENSORS AND ENGINE MANAGEMENT SYSTEM

Programme & Branch	M.E.- Embedded Systems	Sem.	Category	L	T	P	Credit
Prerequisites	NIL	4	PE	3	0	0	3

Preamble	This course enables the students to learn the concepts and analyze the uses of sensors in automotive systems and apply the various novel methods to develop electronic based automobile devices for all vehicle conditions.	
Unit - I	**Introduction:**	**9**
Evolution and Development of electronics in automobiles- Electrical and Electronic Principles – Measurements – Sensors – Thermistors – Thermocouples – Inductive Sensor – Hall Effect – Strain gauge – Variable Capacitive – Variable Resistance – Knock Sensors – LVDT – Hot wire air flow – Thin film air flow – Vortex flow – Pitot tube – Turbine fluid flow sensor – optical sensors – Oxygen sensors – Light sensors – Thick flim air temperature sensor – Methanol – Rain – Oil – Dynamic vehicle position sensor – Actuators – Solenoid Actuators – EGR Valve – Motorized – Stepper motor – Synchronous – Thermal Actuators Standards and Norms – Euro Norms – Bharat Norms – Emission Testing		
Unit - II	**Batteries, Charging and Starting systems:**	**9**
Vehicle batteries requirements, choosing battery and positioning – Lead acid batteries – Maintenance, charging and testing batteries – Working of charging system – Circuit diagram – Rectification methods – Types of Alternators – Smart Charging. Requirements of starting system – Starter motor and Circuits – DC Characteristics – Types of Starter motors		
Unit - III	**Ignition and Injection Systems:**	**9**
Ignition systems: Ignition fundamentals – Electronic ignition systems – Electronic Spark Ignition advance – Distribution less Ignition – Coil on plug ignition – Spark Plugs. Electronic fuel Control – Basics of combustion – Engine fuelling and exhaust emissions – Electronic control of carburetion – Fuel Injection – Petrol fuel injection – Diesel fuel injection.		
Unit - IV	**Engine management system:**	**9**
Combined ignition and fuel systems – Exhaust Emission control – Catalytic converter – EGR – SCR – DeNox Trap – Motronic M3 – DI Motronic – ME Motronic principles – Lean burn engine – 2 stroke engine – Combustion control system – Active Cooling - Engine trends – spark ignition – Transonic combustion – Formula 1 engine technology – Diagnosing engine management systems		
Unit - V	**Chassis, Comfort and Safety Systems:**	**9**
Antilock braking system – Traction and Stability Control – Active Suspension – Electronic control of automatic transmission – Cruise control – Adaptive cruise control – Security – Airbag and Seat belt tensioners. Centralized door locking system – Climate control of cars – Obstacle avoidance Radar – Automatic Parking System. Electric vehicles – Vehicle Layout – Charging system. In vehicle networks: CAN, LIN, FLEXRAY, MOST, KWP2000		

Lecture:45, Total:45

REFERENCES:

1	Tom Denton, Automobile Electrical and Electronics Systems, 4th Edition, Edward Arnold Publishers, London, 2013.
2	Ribbens William B, Understanding Automotive Electronics, 7th Edition, Butterworth- Heinemann, Burlington, 2012.
3	Hollembeak, Barry, Automotive Electricity, Electronics & Computer Controls, Delmar Publishers, New York, 2002.
4	Tim, Gilles, Automotive Engines: Diagnosis, Repair, Rebuilding, 7th Edition, Delmar Publishers, New York, 2015.
5	Donald Christiansen and Charles K. Alexander, Standard Handbook of Electronic Engineering, 5th Edition, McGraw-Hill, 2005.
6	Robert Bosch GmbH, Automotive Hand Book, 9th Edition, Wiley, 2014.
7	Ronald K Jurgen, Automotive Electronics, McGraw Hill, 2nd Edition, 1999.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	adapt to the continuous changes in emission norms of India and uses of sensors and actuators in automobile applications.	Understanding(K2)
CO2	identify the operations of charging and starting techniques involved in Vehicles.	Applying(K3)
CO3	analyze the use of electronic ignition and fuel injection system used in automobile	Applying(K3)
CO4	apply the engine and fuel control system for ECU used in engine management system	Applying(K3)
CO5	employ the essential comfort and safety systems for automobile.	Applying(K3)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	1				
CO2	3	2	1	1		
CO3	3	2	1	1		
CO4	3	2	1	1		
CO5	3	2	1	1		

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1	**40**	**55**	**5**				**100**
CAT2	**30**	**50**	**15**				**100**
CAT3	**20**	**50**	**30**				**100**
ESE	**40**	**40**	**20**				**100**

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

20ESE17 MULTICORE PROCESSOR AND COMPUTING

Programme & Branch	M.E.- Embedded Systems	Sem.	Category	L	T	P	Credit
Prerequisites	NIL	4	PE	3	0	0	3

Preamble	To know the basic knowledge about multiprocessor, multicomputer systems and advanced processor technology in parallel processors	
Unit - I	**MULTI-CORE PROCESSORS:**	**9**
Single core to Multi-core architectures – SIMD and MIMD systems – Interconnection networks - Symmetric and Distributed Shared Memory Architectures – Cache coherence - Performance Issues –Parallel program design.		
Unit - II	**PARALLEL PROGRAM CHALLENGES:**	**9**
Performance – Scalability – Synchronization and data sharing – Data races – Synchronization primitives (mutexes, locks, semaphores, barriers) – deadlocks and live locks – communication between threads (condition variables, signals, message queues and pipes).		
Unit - III	**SHARED MEMORY PROGRAMMING WITH OpenMP:**	**9**
OpenMP Execution Model – Memory Model – OpenMP Directives – Work - sharing Constructs - Library functions – Handling Data and Functional Parallelism – Handling Loops - Performance Considerations.		
Unit - IV	**DISTRIBUTED MEMORY PROGRAMMING WITH MPI:**	**9**
MPI program execution – MPI constructs – libraries – MPI send and receive – Point - to - point and Collective communication – MPI derived data types – Performance evaluation.		
Unit - V	**PARALLEL PROGRAM DEVELOPMENT:**	**9**
Case studies - n - Body solvers – Tree Search –OpenMP and MPI implementations and comparison.		

Lecture: 45, Total: 45

REFERENCES:

1.	Peter S. Pacheco, An Introduction to Parallel Programming, Morgan - Kauffman/Elsevier, 2011
2.	Darryl Gove, Multicore Application Programming for Windows, Linux, and Oracle Solaris,Pearson, 2011
3	Michael J Quinn, Parallel programming in C with MPI and OpenMP, Tata McGraw Hill, 2003
4	Jason Roberts , Shameem Akhter, Multi-core Programming:Increasing Performance through Software Multi-threading, Intel Press, 2006.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	interpret the operations of multiprocessor and multicomputer systems.	Understanding(K2)
CO2	know the advanced processor technology, pipelining and scalable architectures.	Understanding(K2)
CO3	develop programs using OpenMP.	Applying(K3)
CO4	write simple programs for distributed memory in MPI	Applying(K3)
CO5	compare programming for serial processors parallel processors.	Analyzing(K4)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1			3	3		
CO2			3	2		
CO3	2	2	3	2	2	1
CO4	2	2	2	3	2	1
CO5			3	3		2

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1	40	60					100
CAT2	10	40	50				100
CAT3		30	40	30			100
ESE	10	30	40	20			100

*** ±3% may be varied * (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

20ESE18 DSP PROCESSOR ARCHITECTURE AND PROGRAMMING

Programme & Branch	M.E.- Embedded System	Sem.	Category	L	T	P	Credit
Prerequisites	NIL	4	PE	3	0	0	3

Preamble	To get familiar with DSP processor architecture and understand the software tools for implementing the real time applications using Embedded DSP processor	
Unit - I	**Fundamentals of programmable DSPs:**	**9**
Multiplier and Multiplier accumulator (MAC) – Modified Bus Structures and Memory access in Programmable DSPs – Multiple access memory – Multi-port memory – VLIW architecture- Pipelining – Special Addressing modes in P-DSPs – On chip Peripherals		
Unit - II	**TMS320C67XX Architecture:**	**9**
Fundamentals of Programmable DSPs - Architecture of TMS320C67XX - Buses- Computational Units- -On-chip peripherals-Timers and Interrupts		
Unit - III	**TMS320C67XX Programming:**	**9**
Pipeline operation - Address Generation Units-Memory organization- Memory architecture -Addressing modes and instruction set-assembly language instructions specific to filter applications-ASM Statement within C -C-Callable Assembly Function		
Unit - IV	**DSP Development System**	**9**
Introduction -DSK Support Tools - DSK Board TMS320C67XX Digital Signal Processor - Code Composer Studio -CCS Installation and Support -Initialization/Communication File - Vector File- Linker File - Compiler - Assembler –Linker- Input and Output with the DSK- Introduction TLC320AD535 (AD535) Onboard Codec for Input and Output - PCM3003 Stereo Codec for Input and Output - Programming Examples Using C Code		
Unit - V	**Applications Using TMS320C67XX:**	**9**
FIR Filter applications-Adaptive filter Applications-Image Processing Applications- Communication Applications-Modulation (all applications using Simulink Blocksets)		

Lecture:45, Total:45

REFERENCES:

1	Venkataramani, B. and Bhaskar, M. Digital Signal Processors: Architecture, Programming and Applications,2nd Edition,Tata McGraw–Hill, New Delhi, 2010
2	Rulph Chassaing , DSP Applications Using C and the TMS320C6x DSK, 1st Edition, John Wiley & Sons, Interscience 2002
3	TMS320C67x/C67x+ DSP CPU and Instruction Set Reference Guide-Texas Instrumentation, “User guides: www.ti.com

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	infer the basic concepts of DSP processor	Understanding(K2)
CO2	illustrate the basic principles and functions of peripheral units to perform real time operations.	Understanding(K2)
CO3	apply programming concepts to develop simple and real time applications programs using C67XX processor	Applying(K3)
CO4	apply programming concepts to develop simple and real time applications using C67XX DSK with CCS	Applying(K3)
CO5	demonstrate the performance of DSP processors for various domain related applications.	Applying(K3)

Mapping of COs with POs						
COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	2	2	3	3		
CO2	3	3	3	2		
CO3	3	3	3	2		
CO4	3	3	3	2		
CO5		3	3	2		
1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy						

ASSESSMENT PATTERN - THEORY							
Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	30	70					100
CAT2	30	40	30				100
CAT3	30	40	30				100
ESE	30	40	30				100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

20ESE19 DESIGN AND ANALYSIS OF ALGORITHMS

Programme & Branch	M.E.- Embedded Systems	Sem.	Category	L	T	P	Credit
Prerequisites	NIL	4	PE	3	0	0	3

Preamble	To introduce the fundamental concepts of Designing Strategies, Complexity analysis of Algorithms, followed by problems on Graph Theory and Sorting methods and also includes the basic concepts on Complexity theory.	
Unit - I	**Introduction:**	**9**
The Role of Algorithms in Computing- Growth of Functions - Analysis of Recursive and Non-recursive Functions – Lists - Heap Sort – Quick Sort – Sorting in Linear Time.		
Unit - II	**Advanced Data Structures**:	**9**
Binary Search Trees-Red-Black Trees-Augmenting Data Structures - Trees –Fibonacci Heaps		
Unit - III	**Algorithm Design Techniques:**	**9**
Dynamic Programming -Rod cutting -Matrix-chain multiplication - Elements of dynamic programming -Longest common subsequence - Optimal binary search trees. Greedy Algorithms : An activity-selection problem -Elements of the greedy strategy - Huffman codes-Matroids and greedy methods - A task-scheduling problem as a matroid Parallel Algorithms**:** Parallelism introduction- THE PRAM MODEL-Simple parallel operations-Parallel searching, sorting, numerical algorithms-Parallel Graph algorithms		
Unit - IV	**Graph Algorithms:**	**9**
Elementary Graph Algorithms- Minimum Spanning Trees- Single Source Shortest Paths- All-Pairs Shortest Paths-Maximum Flow.		
Unit - V	**Non-Deterministic Algorithms:**	**9**
NP-Completeness: Polynomial Time verification, NP Completeness and Reducibility – NP Completeness Proofs – NP Complete Problems		

Lecture: 45, Total: 45

REFERENCES:

1.	Thomas H, Cormen, Charles E. Leiserson, Ronald L. Rivest and Clifford Stein. Introduction to Algorithms, 3rd Edition, MIT Press, USA, 2009.
2.	Jeffrey J. McConnell Canisius College. Analysis of Algorithms: An Active Learning Approach, Jones and Bartlett Publishers,2007.
3	Aho Alfred V, Hopcroft, John E. and Ulllman, Jeffrey D. Data Structures and Algorithms, Pearson Education, New Delhi, 2002.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	design and implement elementary data structures	Applying(K3)
CO2	design and implement advanced data structures	Applying(K3)
CO3	choose appropriate algorithm design technique and solve problems	Applying(K3)
CO4	implement graph algorithms	Applying(K3)
CO5	Analyze the time and space complexity of algorithms.	Analyzing(K4)

Mapping of COs with POs						
COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1			2	3		
CO2			2	3		
CO3	2		3	2		
CO4	1		3	2	2	
CO5	2		2	3		2
1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy						

ASSESSMENT PATTERN - THEORY							
Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	10	30	20	20	10	10	100
CAT2	10	30	20	20	20		100
CAT3	10	30	20	20	20		100
ESE	10	30	20	20	10	10	100

*** ±3% may be varied * (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

20ESE20 VIRTUAL INSTRUMENTATION FOR INDUSTRIAL APPLICATIONS

Programme & Branch	M.E.- Embedded Systems	Sem.	Category	L	T	P	Credit
Prerequisites	NIL	4	PE	3	0	0	3

Preamble	To impart knowledge about advanced tools in virtual instrumentation to develop new industrial applications	
Unit - I	**GRAPHICAL PROGRAMMING ENVIRONMENT:**	**9**
Introduction- History of Virtual Instrumentation- LabVIEW and VI- Conventional and Graphical Programming - Components of LabVIEW- Tools and Other Palettes- Arranging Objects- Pop-up menus- Color Coding- Code Debugging- Context Sensitive Help- Types of VIs- Creating Sub-VIs.		
Unit - II	**INTRODUCTION to LabVIEW:**	**9**
LabVIEW Environment - Front Panel - Block Diagram - Building GUI - Loops - Execution Structures – Datatypes		
Unit - III	**LabVIEW PROGRAMMING:**	**9**
Arrays - Clusters - Charts - Graphs - Structures - String and File I/O- Data Flow Programming.		
Unit - IV	**DATA ACQUISITION:**	**9**
Instrument Control - GPIB - VISA - Instrument Drivers - DAQ Basics - Signal Conditioning - DAQ Hardware - Analog I/O and Digital I/O - DAQ Assistant - Components of Computer Based Measurement System.		
Unit - V	**EMBEDDED PROGRAMMING WITH LabVIEW:**	**9**
CompactRIO - Setting Up CompactRIO system - Implementing an Embedded Program - Accessing I/O - Interfacing FPGA and Real time processor - Embedded State Machine - Case Study: Temperature Monitor using myRIO.		

Lecture: 45, Total: 45

REFERENCES:

1.	Jovitha Jerome. Virtual Instrumentation using LabVIEW, 3rd Edition, PHI Learning Pvt. Ltd,New Delhi, 2012
2.	Jeffrey Travis, Jim Kring. LabVIEW for Everyone: Graphical Programming Made Easy and Fun, 3rd Edition, Prentice Hall, 2009.
3	NI Resources: https://learn.ni.com/

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	describe the components of LabVIEW and virtual instruments	Understanding(K2)
CO2	describe front panel, block diagram and syntax of LabVIEW	Understanding(K2)
CO3	apply structured programming concepts in developing VI programs	Applying(K3)
CO4	apply knowledge on DAQ tools in practical works	Applying(K3)
CO5	analyze the compact RIO setup for FPGA interfaces.	Analyze(K4)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1			3	2		
CO2			3	2		
CO3	2	1	3	3		
CO4	2	1	3	3		
CO5	2	2	3	3	1	

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1	10	40	60				100
CAT2		20	80				100
CAT3		20	70	10			100
ESE	10	30	50	10			100

*** ±3% may be varied * (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

20GET13 - INNOVATION, ENTREPRENEURSHIP AND VENTURE DEVELOPMENT

Programme & Branch	All ME/MTech, MCA Programmes	Sem.	Category	L	T	P	Credit
Prerequisite	Nil	4	PE	3	0	0	3

Preamble	This course will direct the students on how to employ their innovations towards a successful entrepreneurial venture development.	
UNIT – I	**Innovation and Entrepreneurship:**	**9**
Creativity and Innovation – Types of innovation – challenges in innovation- steps in innovation management- Meaning and concept of entrepreneurship - Role of Entrepreneurship in Economic Development - Factors affecting Entrepreneurship – Entrepreneurship vs Intrapreneurship		
UNIT – II	**Design Thinking and Product Design:**	**9**
Design Thinking and Entrepreneurship – Design Thinking Stages: Empathize – Define – Ideate – Prototype – Test. Design thinking tools: Analogies – Brainstorming – Mind mapping. Techniques and tools for concept generation, concept evaluation – Product architecture –Minimum Viable Product (MVP)- Product prototyping – tools and techniques– overview of processes and materials – evaluation tools and techniques for user-product interaction		
UNIT – III	**Business Model Canvas (BMC) and Business Plan Preparation:**	**9**
Lean Canvas and BMC - difference and building blocks- BMC: Patterns – Design – Strategy – Process–Business model failures: Reasons and remedies. Objectives of a Business Plan - Business Planning Process and Preparation		
UNIT – IV	**IPR and Commercialization:**	**9**
Need for Intellectual Property- Basic concepts - Different Types of IPs: Copy Rights, Trademarks, Patents, Geographical Indications, Trade Secrets and Industrial Design– Patent Licensing - Technology Commercialization – Innovation Marketing		
UNIT – V	**Venture Planning and Means of Finance:**	**9**
Startup Stages - Forms of Business Ownership - Sources of Finance – Idea Grant – Seed Fund – Angel & Venture Fund – Institutional Support to Entrepreneurs – Bank and Institutional Finance to Entrepreneurs		

Total : 45

REFERENCES:

1. Gordon E. & Natarajan K., "Entrepreneurship Development", 6th Edition, Himalaya Publishing House, Mumbai, 2017.
2. Sangeeta Sharma, "Entrepreneurship Development", 1st Edition, PHI Learning Pvt. Ltd., New Delhi, 2017.
3. Charantimath Poornima M., "Entrepreneurship Development and Small Business Enterprises", 3rd Edition, Pearson Education, Noida, 2018.
4. Robert D. Hisrich, Michael P. Peters & Dean A. Shepherd, "Entrepreneurship", 10th Edition, McGraw Hill, Noida, 2018.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1:	understand the relationship between innovation and entrepreneurship	Understanding (K2)
CO2:	understand and employ design thinking process during product design and development	Analysing (K4)
CO3:	develop suitable business models as per the requirement of the customers	Analysing (K4)
CO4:	Practice the procedures for protection of their ideas' IPR	Applying (K3)
CO5:	understand and plan for suitable type of venture and modes of finances	Applying (K3)

Mapping of COs with POs and PSOs			
COs/POs	**PO1**	**PO2**	**PO3**
CO1	3		2
CO2	3		2
CO3	3		2
CO4	3		2
CO5	3		2
1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy			

ASSESSMENT PATTERN - THEORY							
Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	40	40	20				100
CAT2	30	40	30				100
CAT3	30	45	25				100
ESE	30	40	30				100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

20ESE21 TESTING OF VLSI CIRCUITS

Programme & Branch	M.E.- Embedded Systems	Sem.	Category	L	T	P	Credit
Prerequisites	Nil	1	PE	3	0	0	3

Preamble	To know the basics of VLSI test concepts, Test generation, DFT architectures, Built in Self Test and fault diagnosis.	
Unit - I	**Basics of Testing And Fault Modeling:**	**9**
Importance of Testing – Challenges in VLSI testing – Fault Models - Fault detection - Fault location - Fault dominance - Logic Simulation - Types of simulation - Delay models - Gate level Event-driven simulation		
Unit - II	**Design for Testability:**	**9**
Testability analysis -SCOAP Testability Analysis- Probability-Based Testability Analysis - Design for Testability- *Ad Hoc* Approach- Structured Approach - Scan Cell Designs- Scan Architectures - Scan Design Rules		
Unit - III	**Test Generation for Combinational and Sequential Circuits:**	**9**
Random Test generation- Boolean difference method- ATPG for Combinational Circuits- A Basic ATPG Algorithm- D Algorithm- PODEM- FAN- Designing a Sequential ATPG - Time Frame Expansion - 5-Valued Algebra- Designing a Simulation-Based ATPG.		
Unit - IV	**Self-Test and Test Algorithms:**	**9**
Built-In Self Test - Test pattern generation for BIST - BIST Architectures – RAM Functional Fault Models- RAM Functional Fault Models- Functional Test Patterns and Algorithms- March Tests		
Unit - V	**Fault Diagnosis:**	**9**
Logic Level Diagnosis – Fault Dictionary- Diagnosis by UUT reduction - Fault Diagnosis for Combinational Circuits – Effect cause Analysis- Self-checking design.		

Total:45

REFERENCES:

1. Miron Abramovici, Melvin Breuer, Arthur Friedman Digital Systems and Testable Design, 13th Edition, Jaico Publishing House, 2012.
2. Laung – Terng wang, Cheng – wen wu, Xidogingwen, VLSI Testing Principles and Architectures: Design for Testability, 1st Edition, Morgan Kaufmann Publisher, 2013
3. Michael L. Bushnell, Vishwani D. Agrawal, Essentials of Electronic Testing for Digital, Memory and Mixed- Signal VLSI Circuits, 1st Edition, Kluwer Academic Publishers New York, 2002.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	distinguish between different fault models and types of simulation	Understanding (K2)
CO2	identify the design for testability techniques for combinational and sequential circuits	Applying (K3)
CO3	identify the various test generation methods for combinational and sequential circuits	Applying (K3)
CO4	nderstand the various Built In Self Test architectures, memory fault models and testing of memories	Applying (K3)
CO5	review the various fault diagnosis approach for VLSI Systems	Understanding (K2)

Mapping of COs with POs						
COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1			3			
CO2			3		3	
CO3			3		3	
CO4			3			
CO5			3			
1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy						

ASSESSMENT PATTERN - THEORY							
Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	15	45	40				100
CAT2	10	45	45				100
CAT3	15	45	35				100
ESE	20	40	40				100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

20ESE22 APPLICATION SPECIFIC INTEGRATED CIRCUITS

Programme& Branch	M.E-Embedded Systems	Sem.	Category	L	T	P	Credit
Prerequisites	NIL	2	PE	2	0	2	3

Preamble	To know the different programmable ASICs, logic cells, I/O cells and interconnect and to learn how synthesis and physical design flow in carried out in an ASIC design.	
Unit - I	**Introduction to ASICs, CMOS Logic and ASIC Library Design:**	**6**
Types of ASICs - Design flow - Combinational Logic Cell – Sequential logic cell - Transistor Parasitic Capacitance- Logical effort.		
Unit - II	**Programmable ASICs, Programmable ASIC Logic Cells:**	**6**
Anti fuse - static RAM - EPROM and EEPROM technology - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX		
Unit - III	**Programmable ASIC I/O Cells:**	**6**
DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.		
Unit - IV	**Programmable ASIC Interconnect and synthesis:**	**6**
Actel ACT -Xilinx LCA - Xilinx EPLD -.Logic synthesis – Logic Simulation - Design and synthesis of various circuits.		
Unit - V	**Physical Design:**	**6**
ASIC Partitioning - floor planning- placement and routing		

List of Exercises / Experiments :

1.	Design, simulation and synthesis of multipliers
2.	Design, simulation and synthesis of Finite state machine
3.	Design, simulation and synthesis of ALU
4.	Complete the design of two differential amplifiers, one of which uses emitter resistor (R_E) biasing, and one ofwhich uses current mirror biasing.
5.	Analysis of frequency response of current series and current shunt feedback topologies.
6.	Analysis of frequency response of voltage series and voltage shunt feedback topologies

Lecture:30, Practical:30, Total:60

REFERENCES:

1.	Micheal John Sebastian Smith, Application - Specific Integrated Circuits, 12th impression, Pearson,2013
2.	Steve Kilts, “Advanced FPGA Design: Architecture, Implementation, and Optimization” Wiley Inter-Science, 2016
3.	Roger Woods, John McAllister, Gaye Lightbody, Dr. Ying Yi, FPGA-based Implementation of Signal Processing Systems, 2nd Edition, Wiley, 2017

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	demonstrate ASIC Design flow and comprehend the types of ASIC	Understanding(K2)
CO2	realize the issues involved in ASIC design, including design, role of transistor, logical effort and programming technology	Understanding(K2)
CO3	analyze the issues involved in logic cells, I/O cells and interconnect	Analysing(K3)
CO4	perform simulation and synthesis of the design using different programmable ASIC design software	Applying(K3)
CO5	analyze the algorithms used in partitioning, Floorplanning , placement,routing, power and clock design for ASIC	Analyzing(K4)
CO6	perform physical design of digital circuits	Applying(K3), Precision(S3)
CO7	analyze the performance of digital systems	Analyzing (K4), Precision (S3)
CO8	analyse the frequency response of analog circuits	Analyzing (K4), Precision(S3)

Mapping of COs with POs						
COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	2		3			
CO2	2		3			
CO3	2		3	2	2	
CO4	3		3	3	3	3
CO5	3	2	3	3	3	
CO6	3	2	1	1		
CO7	3	2	1	1		
CO8	3	2	1	1		
1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy						

ASSESSMENT PATTERN - THEORY							
Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	20	35	45				100
CAT2	15	35	30	20			100
CAT3	20	20	30	30			100
ESE	15	35	30	20			100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks**

20ESE23 LOW POWER VLSI DESIGN

Programme & Branch	M.E- Embedded Systems	Sem.	Category	L	T	P	Credit
Prerequisites	Nil	3	PE	3	0	0	3

Preamble	To design the combinational and sequential circuits with minimum power consumption and to anlayse the various power optimization methods and techniques to reduce power consumption.	
Unit - I	**Power dissipation in CMOS:**	**9**
Hierarchy of limits of power – Sources of power consumption – Physics of power dissipation in CMOS FET devices – Basic principle of low power design		
Unit - II	**Power optimization :**	**9**
Logic level power optimization – Circuit level low power design – circuit techniques for reducing power consumption in adders and multipliers.		
Unit - III	**Design of Low Power CMOS circuits :**	**9**
Computer arithmetic techniques for low power system – reducing power consumption in memories – low power clock, Inter connect and layout design – Advanced techniques –Special techniques		
Unit - IV	**Power estimation:**	**9**
Power Estimation techniques – logic power estimation – Simulation power analysis –Probabilistic power analysis.		
Unit - V	**Software design for low power :**	**9**
Sources of Software Power dissipation- Power Estimation- Power Optimization- Automated low power code generation- Codesign for low power		

Total:45

REFERENCES:

1	Kaushik Roy, Sarat.C.Prasad, Low power CMOS VLSI circuit design, 1st reprint, Wiley India, 2009.
2	Dimitrios Soudris, Chirstian Pignet, Costas Goutis. Designing CMOS Circuits for Low Power, Kluwer Acaemic Publishers, 2010
3	Gary Yeap, Practical low power digital VLSI design, 1st Edition, Springer Science& Business Media, 1998.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	enumerate the different sources of power dissipation in CMOS	Remembering (K1)
CO2	analyze various power optimization technique at circuit level.	Analyzing (K4)
CO3	design of low power circuits at architecture level	Creating (K6)
CO4	use of Simulation and probabilistic method of power analysis	Analyzing (K4)
CO5	perform power estimation and optimization at programming level	Evaluating (K5)

Mapping of COs with POs						
COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1		3	2			
CO2	2		3			
CO3			3		2	3
CO4		2			3	
CO5		2		3	2	3
1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy						

ASSESSMENT PATTERN - THEORY							
Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	15	40	30	15	-	-	100
CAT2	10	15	20	25	15	15	100
CAT3	10	15	25	25	25	-	100
ESE	10	15	20	25	15	15	100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

20ESE24 COMPUTER AIDED DESIGN OF VLSI CIRCUITS

Programme & Branch	M.E-Embedded Systems	Sem.	Category	L	T	P	Credit
Prerequisites	ASIC	4	PE	3	0	0	3

Preamble	To give an overview of the VLSI physical design and understand CAD algorithms used in VLSI physical design automation field.	
Unit - I	**Design Methodologies:**	**9**
Introduction to VLSI Design methodologies – Review of VLSI Design automation tools –Algorithmic Graph Theory and Computational Complexity –Tractable and Intractable problems – general purpose methods for combinatorial optimization problems		
Unit - II	**Partitioning, Placement and Floor planning :**	**9**
Placement and Partitioning –Circuit representation – Placement algorithms – Partitioning- Partitioning algorithms-Floor planning concepts –shape functions and floor plan sizing –Floorplanning based on Simulated Annealing		
Unit - III	**Routing and Compaction:**	**9**
Routing – Types of local routing problems – Area routing – channel routing – global routing –algorithms for global routing. Compaction- Layout Compaction –Design rules –problem formulation –algorithms for constraint graph compaction.		
Unit - IV	**Logic Simulation**:	**9**
Simulation –Gate-level modeling and simulation –Switch-level modeling and simulation . Introduction to Combinational Logic Synthesis –Binary Decision Diagrams –ROBDD- ROBDD principles, implementation, construction and manipulation.		
Unit - V	**High level Synthesis** :	**9**
Hardware models –Internal representation –Allocation assignment and scheduling –Simple scheduling algorithm –Assignment problem –High level transformations.		

Total:45

REFERENCES:

1	Sabih H. Gerez Algorithms for VLSI Design Automation, John Wiley & Sons, New York, 2002
2	Naveed Sherwani Algorithms for VLSI Physical Design Automation, 3rd Edition, Kluwar Academic Publishers, Boston, 2002
3	Majid Sarrafzadeh, Wong C.K An Introduction to VLSI Physical Design, 2nd Edition, McGraw Hill International Edition 1996

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	comprehend the concepts and properties associated with Graph Theory.	Understanding (K2)
CO2	demonstrate the concepts of Physical Design Process such as partitioning, floor planning, Placement and Routing.	Understanding (K2)
CO3	apply the concepts of design optimization algorithms and their application to VLSI physical design automation.	Applying (K3)
CO4	realize the concepts of simulation and synthesis in VLSI Design automation.	Understanding (K2)
CO5	analyze CAD design problems using algorithmic methods for VLSI physical design automation.	Analyzing (K4)

Mapping of COs with POs						
COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	3		2			
CO2	3		3			
CO3	3		3	3	2	
CO4			3	3	3	
CO5	2	3			3	2
1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy						

ASSESSMENT PATTERN - THEORY							
Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	15	45	40				100
CAT2	10	45	45				100
CAT3	15	45	35				100
ESE	20	40	40				100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**