KONGU ENGINEERING COLLEGE

(Autonomous Institution Affiliated to Anna University, Chennai)

PERUNDURAI ERODE – 638 060

TAMILNADU INDIA

Estd : 1984

REGULATIONS, CURRICULUM & SYLLABI – 2022

(CHOICE BASED CREDIT SYSTEM AND OUTCOME BASED EDUCATION)

(For the students admitted during 2022 - 2023 and onwards)

MASTER OF ENGINEERING DEGREE IN EMBEDDED SYSTEMS

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

KONGU
Assuring the Best

KONGU ENGINEERING COLLEGE, PERUNDURAI, ERODE – 638060
(An Autonomous Institution Affiliated to Anna University)

REGULATIONS 2022

CHOICE BASED CREDIT SYSTEM AND OUTCOME BASED EDUCATION

MASTER OF ENGINEERING (ME) / MASTER OF TECHNOLOGY (MTech) DEGREE PROGRAMMES

These regulations are applicable to all candidates admitted into ME/MTech Degree programmes from the academic year 2022 – 2023 onwards.

1. DEFINITIONS AND NOMENCLATURE

In these Regulations, unless otherwise specified:

i. "University" means ANNA UNIVERSITY, Chennai.

ii. "College" means KONGU ENGINEERING COLLEGE.

iii. "Programme" means Master of Engineering (ME) / Master of Technology (MTech) Degree programme

iv. "Branch" means specialization or discipline of ME/MTech Degree programme, like Construction Engineering and Management, Information Technology, etc.

v. "Course" means a Theory / Theory cum Practical / Practical course that is normally studied in a semester like Engineering Design Methodology, Machine Learning Techniques, etc.

vi. "Credit" means a numerical value allocated to each course to describe the candidate's workload required per week.

vii. "Grade" means the letter grade assigned to each course based on the marks range specified.

viii. "Grade point" means a numerical value (0 to 10) allocated based on the grade assigned to each course.

ix. "Principal" means Chairman, Academic Council of the College.

x. "Controller of Examinations" means authorized person who is responsible for all examination related activities of the College.

xi. "Head of the Department" means Head of the Department concerned of the College.

2. PROGRAMMES AND BRANCHES OF STUDY

The following programmes and branches of study approved by Anna University, Chennai and All India Council for Technical Education, New Delhi are offered by the College.

Programme	Branch
	Structural Engineering
	VLSI Design
	Embedded Systems
	Computer Science and Engineering
MTech	Information Technology
	Food Technology

3. ADMISSION REQUIREMENTS

Candidates seeking admission to the first semester of the ME/MTech Degree programme shall be required to have passed an appropriate qualifying Degree Examination of Anna University or any examination of any other University or authority accepted by the Anna University, Chennai as equivalent thereto, subject to amendments as may be made by the Anna University, Chennai from time to time. The candidates shall also be required to satisfy all other conditions of admission prescribed by the Anna University, Chennai and Directorate of Technical Education, Chennai from time to time.

4. STRUCTURE OF PROGRAMMES

4.1 Categorisation of Courses

The ME / MTechprogramme shall have a curriculum with syllabi comprising of theory, theory cum practical, practical courses in each semester and project work, internship,etc that have been approved by the respective Board of Studies and Academic Council of the College. All the programmes have well defined Programme Outcomes (PO) and Programme Educational Objectives (PEOs) as per Outcome Based Education (OBE). The content of each course is designed based on the Course Outcomes (CO). The courses shall be categorized as follows:

i. Foundation Courses (FC)

ii. Professional Core (PC) Courses

iii. Professional Elective (PE) Courses

iv. Open Elective (OE) Courses

v. Employability Enhancement Courses (EC) like Innovative Project, Internship cum Project work in Industry or elsewhere, Project Work

4.2 Credit Assignment

Each course is assigned certain number of credits as follows:

Contact period per week	Credits
1 Lecture / Tutorial Period	1
2 Practical Periods	1
2 Project Work Periods	1
40 Training /Internship Periods	1

The minimum number of credits to complete the ME/MTechprogramme is 72.

4.3 Employability Enhancement Courses

A candidate shall be offered with the employability enhancement courses like innovative project, internship cum project work and project work during the programme to gain/exhibit the knowledge/skills.

4.3.1 Innovative Project

A candidate shall earn two credits by successfully completing the project by using his/her innovations in second semester during his/her programme.

4.3.2 Internship cum Project Work

The curriculum enables a candidate to go for full time projects through internship during the third semester and can earn credits through it for his/her academics vide clause 7.6 and clause 7.12. Such candidate shall earn the minimum number of credits as mentioned in the third semester of the curriculum other than internship by either fast track mode or through approved courses in online mode or by self study mode. Such candidate can earn the number of credits for the internship same as that of Project Work in the third semester. Assessment procedure is to be followed as specified in the guidelines approved by the Academic Council.

4.3.4 Project Work

A candidate shall earn nine credits by successfully completing the project work in fourth semester during the programme inside the campus or in industries.

4.4 One / Two CreditCourses / Online Courses / Self Study Courses

The candidates may optionally undergo One / Two Credit Courses / Online Courses / Self Study Courses as elective courses.

4.4.1 One / Two Credit Courses: One / Two Credit Courses shall be offered by the college with the prior approval from respective Board of Studies. A candidate can earn a maximum of six credits through one / two credit courses during the entire duration of the programme.

4.4.2 **Online Courses:** Candidates may be permitted to earn credits for online courses, offered by NPTEL / SWAYAM / a University / Other Agencies, approved by respective Board of Studies.

4.4.3 **Self Study Courses:** The Department may offer an elective course as a self study course. The syllabus of the course shall be approved by the respective Board of Studies. However, mode of assessment for a self study course will be the same as that used for other courses. The candidates shall study such courses on their own under the guidance of member of the faculty. Self study course is limited to one per semester.

4.4.4 The elective courses in the final year may be exempted if a candidate earns the required credits vide clause 4.4.1, 4.4.2 and 4.4.3 by registering the required number of courses in advance (up to second semester).

4.4.5 A candidate can earn a maximum of 15 credits through all one /two credit courses, online courses and self study courses.

4.5 Flexibility to Add or Drop Courses

4.5.1 A candidate has to earn the total number of credits specified in the curriculum of the respective programme of study in order to be eligible to obtain the degree. However, if the candidate wishes, then the candidate is permitted to earn more than the total number of credits prescribed in the curriculum of the candidate's programme.

4.5.2 From the second to fourth semesters the candidates have the option of registering for additional elective courses or dropping of already registered additional elective courses within two weeks from the start of the semester. Add / Drop is only an option given to the candidates. Total number of credits of such courses during the entire programme of study cannot exceed eight.

4.6 Maximum number of credits the candidate can enroll in a particular semester cannot exceed 30 credits.

4.7 The blend of different courses shall be so designed that the candidate at the end of the programme would have been trained not only in his / her relevant professional field but also would have developed to become a socially conscious human being.

4.8 The medium of instruction, examinations and project report shall be English.

5. DURATION OF THE PROGRAMME

5.1 A candidate is normally expected to complete the ME / MTech Degree programme in 4 consecutive semesters (2 Years), but in any case not more than 8 semesters (4 Years).

5.2 Each semester shall consist of a minimum of 90 working days including continuous assessment test period. The Head of the Department shall ensure that every teacher imparts instruction as per the number of periods specified in the syllabus for the course being taught.

5.3 The total duration for completion of the programme reckoned from the commencement of the first semester to which the candidate was admitted shall not exceed the maximum duration specified in clause 5.1 irrespective of the period of break of study (vide clause 11) or prevention (vide clause 9) in order that the candidate may be eligible for the award of the degree (vide clause 16). Extension beyond the prescribed period shall not be permitted.

6. COURSE REGISTRATION FOR THE EXAMINATION

6.1 Registration for the end semester examination is mandatory for courses in the current semester as well as for the arrear courses failing which the candidate will not be permitted to move on to the higher semester. This will not be applicable for the courses which do not have an end semester examination.

6.2 The candidates who need to reappear for the courses which have only continuous assessment shall enroll for the same in the subsequent semester, when offered next, and repeat the course. In this case, the candidate shall attend the classes, satisfy the attendance requirements (vide clause 8), earn continuous assessment marks. This will be considered as an attempt for the purpose of classification.

6.3 If a candidate is prevented from writing end semester examination of a course due to lack of attendance, the candidate has to attend the classes, when offered next, and fulfill the attendance requirements as per clause 8 and earn continuous assessment marks. If the course, in which the candidate has a lack of attendance, is an elective, the candidate may register for the same or any other elective course in the subsequent semesters and that will be considered as an attempt for the purpose of classification.

7. ASSESSMENT AND EXAMINATION PROCEDURE FOR AWARDING MARKS

7.1 The ME/MTechprogrammes consist of Theory Courses, Theory cum Practical courses, Practical courses, Innovative Project, Internship cum Project work and Project Work. Performance in each course of study shall be evaluated based on (i) Continuous Assessments (CA) throughout the semester and (ii) End Semester Examination (ESE) at the end of the semester except for the courses which are evaluated based on continuous assessment only. Each course shall be evaluated for a maximum of 100 marks as shown below:

<table>
<tr><th>Sl. No.</th><th>Category of Course</th><th>Continuous Assessment Marks</th><th>End Semester Examination Marks</th></tr>
<tr><td>1.</td><td>Theory</td><td>40</td><td>60</td></tr>
<tr><td>2.</td><td>Theory cum Practical (The distribution of marks shall be</td><td>50</td><td>50</td></tr>
<tr><td>3.</td><td>Practical</td><td>60</td><td>40</td></tr>
<tr><td>4.</td><td>Project Work / Internship cum Project Work</td><td>50</td><td>50</td></tr>
<tr><td>5.</td><td>One / Two credit Course</td><td rowspan="2">The distribution of marks shall be decided based on the credit weightage assigned</td><td rowspan="2">---</td></tr>
<tr><td>6.</td><td>All other Courses</td></tr>
</table>

7.2 Examiners for setting end semester examination question papers for theory courses, theory cum practical courses and practical courses and evaluating end semester examination answer scripts, project works, innovative project and internships shall be appointed by the Controller of Examinations after obtaining approval from the Principal.

7.3 Theory Courses

For all theory courses out of 100 marks, the continuous assessment shall be 40 marks and the end semester examination shall be for 60 marks. However, the end semester examinations shall be conducted for 100 marks and the marks obtained shall be reduced to 50. The continuous assessment tests shall be conducted as per the schedule laid down in the academic schedule. Three tests shall be conducted for 50 marks each and reduced to 30 marks each. The total of the continuous assessment marks and the end semester examination marks shall be rounded off to the nearest integer.

7.3.1 The assessment pattern for awarding continuous assessment marks shall be as follows:

Sl. No.	Type	Max. Marks	Remarks
1.	Test - I	12.5	---
	Test - II	12.5	
2.	Tutorial / Others (Tutorial/Problem Solving (or) Simulation (or) Simulation & Mini Project (or) Mini Project (or) Case Studies (or) Any other relevant to the course)	10	Type of assessment is to be chosen based on the nature of the course and to be approved by Principal
3.	Assignment / Paper Presentation in Conference / Seminar / Comprehension / Activity based learning / Class notes	05	To be assessed by the Course Teacher based on any one type.
	Total	40	Rounded off to the one decimal place

However, the assessment pattern for awarding the continuous assessment marks may be changed based on the nature of the course and is to be approved by the Principal.

7.3.2 A reassessment test or tutorial covering the respective test or tutorial portions may be conducted for those candidates who were absent with valid reasons (Sports or any other reason approved by the Principal).

7.3.3 The end semester examination for theory courses shall be for duration of three hours and shall be conducted between November and January during odd semesters and between April and June during even semesters of every year.

7.4 Theory cum Practical Courses

For courses involving theory and practical components, the evaluation pattern as per the clause 7.1 shall be followed. Depending on the nature of the course, the end semester examination shall be conducted for theory and the practical components. The apportionment of continuous assessment and end semester examination marks shall be decided based on the credit weightage assigned to theory and practical components approved by Principal.

7.5 Practical Courses

For all practical courses out of 100 marks, the continuous assessment shall be for 50 marks and the end semester examination shall be for 50 marks. Every exercise / experiment shall be evaluated based on the candidate's performance during the practical class and the candidate's records shall be maintained.

7.5.1 The assessment pattern for awarding continuous assessment marks for each course shall be decided by the course coordinator based on rubrics of that particular course, and shall be based on rubrics for each experiment.

7.5.2 The end semester examination shall be conducted for a maximum of 100 marks for duration of 3 hours and reduced to 40 marks. The appointment of examiners and the schedule shall be decided by chairman of Board of Study of the relevant board.

7.6 Project Work

7.6.1 Project work shall becarried out individually. Candidates can opt for full time internship (vide clause 7.7) in lieu of project work in third semester. The project work is mandatory for all the candidates.

7.6.2 The Head of the Department shall constitute review committee for project work. There shall be two assessments by the review committee during the semester. The candidate shall make presentation on the progress made by him/her before the committee.

7.6.3 The continuous assessment and end semester examination marks for Project Work and the Viva-Voce Examination shall be distributed as below.

Continuous Assessment (Max. 50 Marks)						End Semester Examination (Max. 50 Marks)			
Review I (Max..10 Marks)		Review II (Max.. 20 Marks)		Review III (Max. 20 Marks)		Report Evaluation (Max. 20 Marks)	Viva - Voce (Max. 30 Marks)		
Rv. Com	Guide	Review Committee (excluding guide)	Guide	Review Committee (excluding guide)	Guide	Ext. Exr.	Guide	Exr.1	Exr.2
5	5	10	10	10	10	20	10	10	10

7.6.4 The Project Report prepared according to approved guidelines and duly signed by the Supervisor shall be submitted to Head of the Department. A candidate must submit the project report within the specified date as per the academic schedule of the semester. If the project report is not submitted within the specified date then the candidate is deemed to have failed in the Project Work and redo it in the subsequent semester. This applies to both Internship cum Project work and Project work.

7.6.5 If a candidate fails to secure 50% of the continuous assessment marks in the project work, he / she shall not be permitted to submit the report for that particular semester and shall have to redo it in the subsequent semester and satisfy attendance requirements.

7.6.6 Every candidate shall, based on his/her project work, publish a paper in a reputed journal or reputed conference in which full papers are published after usual review. A copy of the full paper accepted and proof for that shall be produced at the time of evaluation.

7.6.7 The project work shall be evaluated based on the project report submitted by the candidate in the respective semester and viva-voce examination by a committee consisting of two examiners and guide of the project work.

7.6.8 If a candidate fails to secure 50 % of the end semester examination marks in the project work, he / she shall be required to resubmit the project report within 30 days from the date of declaration of the results and a fresh viva-voce examination shall be conducted as per clause 7.6.7.

7.6.9 A copy of the approved project report after the successful completion of viva-voce examination shall be kept in the department library.

7.7 Internship cum Project Work

Each candidate shall submit a brief report about the internship undergone and a certificate issued from the organization concerned at the time of Viva-voce examination to the review committee. The evaluation method shall be same as that of the Project Work as per clause 7.6 excluding 7.6.6.

7.8 One / Two Credit Course

Two assessments shall be conducted during the value added course duration by the offering department concerned.

7.9 Online Course

The Board of Studies will provide methodology for the evaluation of the online courses. The Board can decide whether to evaluate the online courses through continuous assessment and end semester examination or through end semester examination only. In case of credits earned through online mode from NPTEL / SWAYAM / a University / Other Agencies approved by Chairman, Academic Council, the credits may be transferred and grades shall be assigned accordingly.

7.10 Self Study Course

The member of faculty approved by the Head of the Department shall be responsible for periodic monitoring and evaluation of the course. The course shall be evaluated through continuous assessment and end semester examination. The evaluation methodology shall be the same as that of a theory course.

7.11 Audit Course

A candidate may be permitted to register for specific course not listed in his/her programme curriculum and without undergoing the rigors of getting a 'good' grade, as an Audit course, subject to the following conditions.

The candidate can register only one Audit course in a semester starting from second semester subject to a maximum of two courses during the entire programme of study. Such courses shall be indicated as 'Audit' during the time of Registration itself. Only courses currently offered for credit to the candidates of other branches can be audited.

A course appearing in the curriculum of a candidate cannot be considered as an audit course. However, if a candidate has already met the Professional Elective and Open Elective credit requirements as stipulated in the curriculum, then, a Professional Elective or an Open Elective course listed in the curriculum and not taken by the candidate for credit can be considered as an audit course.

Candidates registering for an audit course shall meet all the assessment and examination requirements (vide clause 7.3) applicable for a credit candidate of that course. Only if the candidate obtains a performance grade, the course will be listed in the semester Grade Sheet and in the Consolidated Grade Sheet along with the grade SC (Successfully Completed). Performance grade will not be shown for the audit course.

Since an audit course has no grade points assigned, it will not be counted for the purpose of GPA and CGPA calculations.

8. REQUIREMENTS FOR COMPLETION OF A SEMESTER

8.1 A candidate who has fulfilled the following conditions shall be deemed to have satisfied the requirements for completion of a semester and permitted to appear for the examinations of that semester.

8.1.1 Ideally, every candidate is expected to attend all classes and secure 100 % attendance. However, a candidate shall secure not less than 80 % (after rounding off to the nearest integer) of the overall attendance taking into account the total number of working days in a semester.

8.1.2 A candidate who could not satisfy the attendance requirements as per clause 8.1.1 due to medical reasons (hospitalization / accident / specific illness) but has secured not less than 70 % in the current semester may be permitted to appear for the current semester examinations with the approval of the Principal on payment of a condonation fee as may be fixed by the authorities from time to time. The medical certificate needs to be submitted along with the leave application. A candidate can avail this provision only twice during the entire duration of the degree programme.

8.1.3 In addition to clause 8.1.1 or 8.1.2, a candidate shall secure not less than 60 % attendance in each course.

8.1.4 A candidate shall be deemed to have completed the requirements of study of any semester only if he/she has satisfied the attendance requirements (vide clause 8.1.1 to 8.1.3) and has registered for examination by paying the prescribed fee.

8.1.5 Candidate's progress is satisfactory.

8.1.6 Candidate's conduct is satisfactory and he/she was not involved in any indisciplined activities in the current semester.

8.2. The candidates who do not complete the semester as per clauses from 8.1.1 to 8.1.6 except 8.1.3 shall not be permitted to appear for the examinations at the end of the semester and not be permitted to go to the next semester. They have to repeat the incomplete semester in next academic year.

8.3 The candidates who satisfy the clause 8.1.1 or 8.1.2 but do not complete the course as per clause 8.1.3 shall not be permitted to appear for the end semester examination of that course alone. They have to repeat the incomplete course in the subsequent semester when it is offered next.

9. REQUIREMENTS FOR APPEARING FOR END SEMESTER EXAMINATION

9.1 A candidate shall normally be permitted to appear for end semester examination of the current semester if he/she has satisfied the semester completion requirements as per clause 8, and has registered for examination in all courses of that semester. Registration is mandatory for current semester examinations as well as for arrear examinations failing which the candidate shall not be permitted to move on to the higher semester.

9.2 When a candidate is deputed for a National / International Sports event during End Semester examination period, supplementary examination shall be conducted for such a candidate on return after participating in the event within a reasonable period of time. Such appearance shall be considered as first appearance.

9.3 A candidate who has already appeared for a course in a semester and passed the examination is not entitled to reappear in the same course for improvement of letter grades / marks.

10. PROVISION FOR WITHDRAWAL FROM EXAMINATIONS

10.1 A candidate may, for valid reasons, be granted permission to withdraw from appearing for the examination in any regular course or all regular courses registered in a particular semester. Application for withdrawal is permitted only once during the entire duration of the degree programme.

10.2 The withdrawal application shall be valid only if the candidate is otherwise eligible to write the examination (vide clause 9) and has applied to the Principal for permission prior to the last examination of that semester after duly recommended by the Head of the Department.

10.3 The withdrawal shall not be considered as an appearance for deciding the eligibility of a candidate for First Class with Distinction/First Class.

10.4 If a candidate withdraws a course or courses from writing end semester examinations, he/she shall register the same in the subsequent semester and write the end semester examinations. A final semester candidate who has withdrawn shall be permitted to appear for supplementary examination to be conducted within reasonable time as per clause 14.

10.5 The final semester candidate who has withdrawn from appearing for project viva-voce for genuine reasons shall be permitted to appear for supplementary viva-voce examination within reasonable time with proper application to Controller of Examinations and on payment of prescribed fee.

11. PROVISION FOR BREAK OF STUDY

11.1 A candidate is normally permitted to avail the authorised break of study under valid reasons (such as accident or hospitalization due to prolonged ill health or any other valid reasons) and to rejoin the programme in a later semester. He/She shall apply in advance to the Principal, through the Head of the Department, stating the reasons therefore, in any case, not later than the last date for registering for that semester examination. A candidate is permitted to avail the authorised break of study only once during the entire period of study for a maximum period of one year. However, in extraordinary situation the candidate may apply for additional break of study not exceeding another one year by paying prescribed fee for the break of study.

11.2 The candidates permitted to rejoin the programme after break of study / prevention due to lack of attendance shall be governed by the rules and regulations in force at the time of rejoining.

11.3 The candidates rejoining in new Regulations shall apply to the Principal in the prescribed format through Head of the Department at the beginning of the readmitted semester itself for prescribing additional/equivalent courses, if any, from any semester of the regulations in-force, so as to bridge the curriculum in-force and the old curriculum.

11.4 The total period of completion of the programme reckoned from the commencement of the semester to which the candidate was admitted shall not exceed the maximum period specified in clause 5 irrespective of the period of break of study in order to qualify for the award of the degree.

11.5 If any candidate is prevented for want of required attendance, the period of prevention shall not be considered as authorized break of study.

11.6 If a candidate has not reported to the college for a period of two consecutive semesters without any intimation, the name of the candidate shall be deleted permanently from the college enrollment. Such candidates are not entitled to seek readmission under any circumstances.

12. PASSING REQUIREMENTS

12.1 A candidate who secures not less than 50 % of total marks (continuous assessment and end semester examination put together) prescribed for the course with a minimum of 45 % of the marks prescribed for the end semester examination in all category of courses vide clause 7.1 except for the courses which are evaluated based on continuous assessment only shall be declared to have successfully passed the course in the examination.

12.2 A candidate who secures not less than 50 % in continuous assessment marks prescribed for the courses which are evaluated based on continuous assessment only shall be declared to have successfully passed the course. If a candidate secures less than 50% in the continuous assessment marks, he / she shall have to re-enroll for the same in the subsequent semester and satisfy the attendance requirements.

12.3 For a candidate who does not satisfy the clause 12.1, the continuous assessment marks secured by the candidate in the first attempt shall be retained and considered valid for subsequent attempts. However, from the fourth attempt onwards the marks scored in the end semester examinations alone shall be considered, in which case the candidate shall secure minimum 50 % marks in the end semester examinations to satisfy the passing requirements, but the grade awarded shall be only the lowest passing grade irrespective of the marks secured.

13. REVALUATION OF ANSWER SCRIPTS

A candidate shall apply for a photocopy of his / her semester examination answer script within a reasonable time from the declaration of results, on payment of a prescribed fee by submitting the proper application to the Controller of Examinations. The answer script shall be pursued and justified jointly by a faculty member who has handled the course and the course coordinator and recommended for revaluation. Based on the recommendation, the candidate can register for revaluation through proper application to the Controller of Examinations. The Controller of Examinations will arrange for revaluation and the results will be intimated to the candidate concerned. Revaluation is permitted only for Theory courses and Theory cum Practical courses where end semester examination is involved.

14. SUPPLEMENTARY EXAMINATION

If a candidate fails to clear all courses in the final semester after the announcement of final end semester examination results, he/she shall be allowed to take up supplementary examinations to be conducted within a reasonable time for the courses of final semester alone, so that he/she gets a chance to complete the programme.

15. AWARD OF LETTER GRADES

For all the passed candidates, the relative grading principle is applied to assign the letter grades.

Marks / Examination Status	Letter Grade	Grade Point
Based on the relative grading	O (Outstanding)	10
	A+ (Excellent)	9
	A (Very Good)	8
	B+ (Good)	7
	B (Average)	6
	C (Satisfactory)	5
Less than 50	U (Reappearance)	0
Successfully Completed	SC	0
Withdrawal	W	-
Absent	AB	-
Shortage of Attendance in a course	SA	-

The Grade Point Average (GPA) is calculated using the formula:

$$GPA = \frac{\sum[(\text{course credits}) \times (\text{grade points})] \text{ for all courses in the specific semester}}{\sum(\text{course credits}) \text{for all courses in the specific semester}}$$

The Cumulative Grade Point Average (CGPA) is calculated from first semester (third semester for lateral entry candidates) to final semester using the formula

$$CGPA = \frac{\sum[(\text{course credits}) \times (\text{grade points})] \text{ for all courses in all the semesters so far}}{\sum(\text{course credits}) \text{for all courses in all the semesters so far}}$$

The GPA and CGPA are computed only for the candidates with a pass in all the courses.

The GPA and CGPA indicate the academic performance of a candidate at the end of a semester and at the end of successive semesters respectively.

A grade sheet for each semester shall be issued containing Grade obtained in each course, GPA and CGPA.

A duplicate copy, if required can be obtained on payment of a prescribed fee and satisfying other procedure requirements.

Withholding of Grades: The grades of a candidate may be withheld if he/she has not cleared his/her dues or if there is a disciplinary case pending against him/her or for any other reason.

16. ELIGIBILITY FOR THE AWARD OF DEGREE

A candidate shall be declared to be eligible for the award of the ME / MTech Degree provided the candidate has

i. Successfully completed all the courses under the different categories, as specified in the regulations.

ii. Successfully gained the required number of total credits as specified in the curriculum corresponding to the candidate's programme within the stipulated time (vide clause 5).

iii. Successfully passed any additional courses prescribed by the respective Board of Studies whenever readmitted under regulations other than R-2020 (vide clause 11.3)

iv. No disciplinary action pending against him / her.

17. CLASSIFICATION OF THE DEGREE AWARDED

17.1 First Class with Distinction:

17.1.1 A candidate who qualifies for the award of the degree (vide clause 16) and who satisfies the following conditions shall be declared to have passed the examination in First class with Distinction:

- Should have passed the examination in all the courses of all the four semestersin the **First Appearance** within four consecutive semesters excluding the authorized break of study (vide clause 11) after the commencement of his / her study.
- Withdrawal from examination (vide clause 10) shall not be considered as an appearance.
- Should have secured a CGPA of not less than 8.50

(OR)

17.1.2 Acandidate who joins from other institutions on transfer or a candidate who gets readmitted and has to move from one regulation to another regulation and who qualifies for the award of the degree (vide clause 16) and satisfies the following conditions shall be declared to have passed the examination in First class with Distinction:

- Should have passed the examination in all the courses of all the four semesters in the **First Appearance** within four consecutive semesters excluding the authorized break of study (vide clause 11) after the commencement of his / her study.
- Submission of equivalent course list approved by the respective Board of studies.
- Withdrawal from examination (vide clause 10) shall not be considered as an appearance.
- Should have secured a CGPA of not less than 9.00

17.2 First Class:

A candidate who qualifies for the award of the degree (vide clause 16) and who satisfies the following conditions shall be declared to have passed the examination in First class:

- Should have passed the examination in all the courses of all four semesters within six consecutive semesters excluding authorized break of study (vide clause 11) after the commencement of his / her study.
- Withdrawal from the examination (vide clause 10) shall not be considered as an appearance.
- Should have secured a CGPA of not less than 6.50

17.3 Second Class:

All other candidates (not covered in clauses 17.1 and 17.2) who qualify for the award of the degree (vide clause 16) shall be declared to have passed the examination in Second Class.

17.4 A candidate who is absent for end semester examination in a course / project work after having registered for the same shall be considered to have appeared for that examination for the purpose of classification.

18. MALPRACTICES IN TESTS AND EXAMINATIONS

If a candidate indulges in malpractice in any of the tests or end semester examinations, he/she shall be liable for punitive action as per the examination rules prescribed by the college from time to time.

19. AMENDMENTS

Notwithstanding anything contained in this manual, the Kongu Engineering College through the Academic council of the Kongu Engineering College, reserves the right to modify/amend without notice, the Regulations, Curricula, Syllabi, Scheme of Examinations, procedures, requirements, and rules pertaining to its ME / MTechprogramme.

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M.E EMBEDDED SYSTEMS CURRICULUM – R2022
(For the students admitted from the academic year 2022-23 onwards)

SEMESTER – I									
Course Code	**Course Title**	**Hours / Week**			**Credit**	**Maximum Marks**			**Category**
		L	**T**	**P**		**CA**	**ESE**	**Total**	
Theory/Theory with Practical									
22AMT12	Applied Mathematics for Electronics Engineers	3	1	0	4	40	60	100	FC
22GET11	Introduction to Research	2	1	0	3	40	60	100	FC
22VLT11	Advanced Digital System Design	3	1	0	4	40	60	100	PC
22ESC11	Verilog HDL For Embedded FPGA Processor	2	0	2	3	50	50	100	PC
22EST11	Microcontroller System Design	3	0	0	3	40	60	100	PC
22EST12	Programming Languages for Embedded Systems	3	0	0	3	40	60	100	PC
Practical / Employability Enhancement									
22ESL11	Microcontroller System Design Laboratory	0	0	2	1	60	40	100	PC
22ESL12	Programming Languages for Embedded Systems Laboratory	0	0	2	1	60	40	100	PC
Total Credits to be earned					22				

SEMESTER – II									
Course Code	**Course Title**	**Hours / Week**			**Credit**	**Maximum Marks**			**Category**
		L	**T**	**P**		**CA**	**ESE**	**Total**	
Theory/Theory with Practical									
22EST21	Embedded Networking and Buses	3	0	0	3	40	60	100	PC
22EST22	Single Board Computer	3	0	0	3	40	60	100	PC
22ESC21	Embedded Linux	3	0	2	4	50	50	100	PC
	Professional Elective - I	3	0	0	3	40	60	100	PE
	Professional Elective - II	3	0	0	3	40	60	100	PE
	Professional Elective - III	3	0	0	3	40	60	100	PE
Practical / Employability Enhancement									
22ESL21	Single Board Computer Laboratory	0	0	2	1	60	40	100	PC
22ESL22	Embedded Networking and Buses Laboratory	0	0	2	1	60	40	100	PC
Total Credits to be earned					21				

M.E EMBEDDED SYSTEMS CURRICULUM – R2022
(For the students admitted from the academic year 2022-23 onwards)

SEMESTER – III									
Course Code	**Course Title**	**Hours / Week**			**Credit**	**Maximum Marks**			**Category**
		L	**T**	**P**		**CA**	**ESE**	**Total**	
Theory/Theory with Practical									
	Professional Elective - IV	3	0	0	3	40	60	100	PE
	Professional Elective - V	3	0	0	3	40	60	100	PE
	Professional Elective - VI	3	0	0	3	40	60	100	PE
Practical / Employability Enhancement									
22ESP31	Project Work - I	0	0	16	8	50	50	100	EC
Total Credits to be earned					17				

SEMESTER – IV									
Course Code	**Course Title**	**Hours / Week**			**Credit**	**Maximum Marks**			**Category**
		L	**T**	**P**		**CA**	**ESE**	**Total**	
Practical / Employability Enhancement									
22ESP41	Project Work - II	0	0	24	12	50	50	100	EC
Total Credits to be earned					12				

Total Credits : 72

LIST OF PROFESSIONAL ELECTIVES (PEs)						
S. No.	**Course Code**	**Course Name**	**L**	**T**	**P**	**C**
Semester - II						
Elective – I						
1.	22VLE01	Testing of VLSI Circuits	3	0	0	3
2.	22ESE01	Distributed Embedded Computing	3	0	0	3
3.	22ESE02	Solar and Energy Storage System	3	0	0	3
Elective – II						
4.	22ESF01	ASIC For Embedded Systems	2	0	2	3
5.	22ESE04	QT Cross Compiling Application Development	3	0	0	3
6.	22ESE05	Sensors and Actuators For Robotics	3	0	0	3
Elective - III						
7.	22ESE06	Signal and Image Processing for Real Time Applications	3	0	0	3
8.	22VLE04	Low Power VLSI Design	3	0	0	3
9.	22ESE07	RTOS for Embedded System	3	0	0	3
Semester - III						
Elective – IV						
10.	22ESE08	Multicore Processor and Computing	3	0	0	3
11.	22ESE09	Virtual Instrumentation for Industrial Applications	3	0	0	3
12.	22ESE10	Wireless Sensor Networks	3	0	0	3
Elective - V						
13.	22ESE11	Programming Internet of Things	3	0	0	3
14.	22ESE12	System on Chip for Embedded Applications	3	0	0	3
15.	22ESE13	Sensors and Engine Management System	3	0	0	3
Elective - VI						
16.	22ESE14	Nature Inspired Optimization Techniques	3	0	0	3
17.	22VLE17	Supervised Machine Learning Algorithms	3	0	0	3
18.	22ESE03	Design of Embedded Systems	3	0	0	3
19.	22GET13	Innovation, Entrepreneurship and Venture Development	3	0	0	3

22AMT12 - APPLIED MATHEMATICS FOR ELECTRONICS ENGINEERS							
Programme& Branch	**M.E &Embedded Systems**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**1**	**FC**	**3**	**1**	**0**	**4**

Preamble	This course will demonstrate various analytical skills in applied mathematics and use extensive mathematical tools such as linear programming, matrix factorizations and queuing theory with the tactics of problem solving and logical thinking applicable in electronics engineering.	
Unit – I	**Advanced Matrix Theory**:	**9+3**
Positive definite matrices – Cholesky decomposition – Generalized Eigenvectors – QR factorization – Generalized inverses – Singular value decomposition –Least squares solution.		
Unit – II	**Vector Spaces:**	**9+3**
Vector Space – Subspaces – Linear dependence and independence – Basis and dimension – Row space, Column space and Null Space – Rank and nullity.		
Unit – III	**Linear Programming:**	**9+3**
Mathematical Formulation of LPP – Basic definitions – Solutions of LPP: Graphical method – Simplex method – Transportation Model – Mathematical Formulation – Initial Basic Feasible Solution: North west corner rule – Vogel's approximation method – Optimum solution by MODI method – Assignment Model – Mathematical Formulation – Hungarian algorithm.		
Unit – IV	**Non-Linear Programming**:	**9+3**
Formulation of non-linear programming problem – Constrained optimization with equality constraints – Constrained optimization with inequality constraints – Graphical method of non–linear programming problem involving only two variables.		
Unit – V	**Queuing Theory:**	**9+3**
Markovian queues – Single and Multi-server Models – Little's formula – Non- Markovian Queues – PollaczekKhintchine Formula.		
Lecture:45, Tutorial:15, Total:60		

REFERENCES/MANUAL/SOFTWARE:

1.	Bronson, R., "Schaum's Outline Series of Matrix Operations", 2nd Edition, McGraw-Hill Education, 2011.
2.	Howard Anton, Anton Kaul, "Elementary Linear Algebra" 12th Edition, John Wiley & Sons, 2019.
3.	KantiSwarup, Gupta, P.K and Man Mohan "Operations Research", 20th Revised Edition, Sultan Chand and Sons., New Delhi, 2019.

COURSE OUTCOMES: On completion of the course, the students will be able to		BT Mapped (Highest Level)
CO1	apply various methods in matrix theory in communication engineering problems.	Applying (K3)
CO2	apply the concepts of linear algebra to solve practical problems.	Applying (K3)
CO3	formulate mathematical models for linear programming problems and solve the transportation and assignment problems.	Applying (K3)
CO4	use non-linear programming concepts in real life situations.	Applying (K3)
CO5	identify the suitable queuing model to handle communication problems.	Applying (K3)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3					
CO2	3					
CO3	3			2	2	
CO4	3			3	3	
CO5	3			3		

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1	10	30	60	-	-	-	100
CAT2	10	20	70	-	-	-	100
CAT3	10	20	70	-	-	-	100
ESE	10	30	60	-	-	-	100

* ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)

22GET11 - INTRODUCTION TO RESEARCH							
(Common to all ME / MTech Branches & MCA)							
Programme& Branch	**All ME/MTech branches & MCA**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**NIL**	**1 / 2**	**FC**	**2**	**1**	**0**	**3**

Preamble	This course will familiarize the fundamental concepts/techniques adopted in research, problem formulation and patenting. Also will disseminate the process involved in collection, consolidation of published literature and rewriting them in a presentable form using latest tools.	
Unit - I	**Concept of Research:**	**6+3**
Meaning and Significance of Research: Skills, Habits and Attitudes for Research - Time Management - Status of Research in India. Why, How and What a Research is? - Types and Process of Research - Outcome of Research - Sources of Research Problem - Characteristics of a Good Research Problem - Errors in Selecting a Research Problem - Importance of Keywords - Literature Collection – Analysis - Citation Study - Gap Analysis - Problem Formulation Techniques.		
Unit - II	**Research Methods and Journals:**	**6+3**
Interdisciplinary Research - Need for Experimental Investigations - Data Collection Methods - Appropriate Choice of Algorithms / Methodologies / Methods - Measurement and Result Analysis - Investigation of Solutions for Research Problem - Interpretation - Research Limitations. Journals in Science/Engineering - Indexing and Impact factor of Journals - Citations - h Index - i10 Index - Journal Policies - How to Read a Published Paper - Ethical issues Related to Publishing - Plagiarism and Self-Plagiarism.		
Unit - III	**Paper Writing and Research Tools:**	**6+3**
Types of Research Papers - Original Article/Review Paper/Short Communication/Case Study - When and Where to Publish? - Journal Selection Methods. Layout of a Research Paper - Guidelines for Submitting the Research Paper - Review Process - Addressing Reviewer Comments. Use of tools / Techniques for Research - Hands on Training related to Reference Management Software - EndNote, Software for Paper Formatting like LaTeX/MS Office. Introduction to Origin, SPSS, ANOVA etc., Software for detection of Plagiarism.		
Unit - IV	**Effective Technical Thesis Writing/Presentation:**	**6+3**
How to Write a Report - Language and Style - Format of Project Report - Use of Quotations - Method of Transcription Special Elements: Title Page - Abstract - Table of Contents - Headings and Sub-Headings - Footnotes - Tables and Figures - Appendix - Bibliography etc. - Different Reference Formats. Presentation using PPTs.		
Unit - V	**Nature of Intellectual Property:**	**6+3**
Patents - Designs - Trade and Copyright. Process of Patenting and Development: Technological research - innovation - patenting - development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents.		
		Lecture: 30, Tutorial:15, Total:45

REFERENCES:

1.	DePoy, Elizabeth, and Laura N. Gitlin, “Introduction to Research-E-Book: Understanding and Applying Multiple Strategies”, Elsevier Health Sciences, 2015.
2.	Walliman, Nicholas, “Research Methods: The basics”, Routledge, 2017.
3.	Bettig Ronald V., “Copyrighting culture: The political economy of intellectual property”, Routledge, 2018.

COURSE OUTCOMES: **On completion of the course, the students will be able to**		**BT Mapped (Highest Level)**
CO1	list the various stages in research and categorize the quality of journals.	Analyzing (K4)
CO2	formulate a research problem from published literature/journal papers	Evaluating (K5)
CO3	write, present a journal paper/ project report in proper format	Creating (K6)
CO4	select suitable journal and submit a research paper.	Applying (K3)
CO5	compile a research report and the presentation	Applying (K3)

Mapping of COs with POs and PSOs

COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**
CO1	3	2	1		
CO2	3	2	3		
CO3	3	3	1		
CO4	3	2	1		
CO5	3	2	1		

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying(K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1		30	40	30			100
CAT2		30	40	30			100
CAT3			30	40	30		100
ESE		30	40	30			100

* ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)

22VLT11- ADVANCED DIGITAL SYSTEM DESIGN							
(Common to VLSI Design and Embedded Systems branches)							
Programme & Branch	**ME - VLSI DESIGN & Embedded Systems**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**1**	**PC**	**3**	**1**	**0**	**4**

Preamble	To design synchronous, asynchronous digital circuits and implement using ASM chart and PLDs	
Unit- I	**Synchronous Sequential Circuit Design:**	9+3
Analysis of Clocked Synchronous Sequential Networks (CSSN) – Modeling of CSSN – State table Reduction –Stable Assignment – Complete Design of CSSN.		
Unit- II	**Algorithmic State Machine (ASM):**	9+3
ASM **–** ASM Chart – Synchronous Sequential Network Design Using ASM Charts – State Assignment –ASM Tables – ASM Realization - Asynchronous Inputs.		
Unit- III	**Asynchronous Circuit Design:**	9+3
Analysis of Asynchronous Sequential Circuit (ASC) - Flow Table Reduction - Racesin ASC – State Assignment Problem and the Transition Table – Design of ASC- Static and Dynamic Hazards – Essential Hazards.		
Unit- IV	**Programming Logic Arrays:**	9+3
PLA minimization – Essential Prime Cube theorem – PLA folding – foldable compatibility matrix - The Compact Algorithm. Practical PLA's – Data Synchronizers – Designing Vending Machine Controller.		
Unit- V	**Programmable Devices:**	9+3
Programmable Logic Devices – Designing a Synchronous Sequential Circuit using a PAL - Realization State machine using PLD Language – FPGAs – ActelACT.		
Lecture:45, Tutorial:15, Total:60		

REFERENCES:

1.	Givone Donald G,"Digital Principles and Design" 1st Edition , McGraw Hill India, reprint 2017.
2.	Yarbrough, JohnM.,"Digital Logic Applications and Design",Cengage Learning India,1st Edition, reprint 2009
3.	BiswasNripendraN,"Logic Design Theory", Prentice Hall of India, New Delhi, reprint 2006.

COURSE OUTCOMES: **On completion of the course, the students will be able to**		**BT Mapped (Highest Level)**
CO1	design clocked synchronous sequential circuits using state table reduction and assignment	Applying (K3)
CO2	realize functions using algorithmic state machines	Applying (K3)
CO3	design the asynchronous sequential circuit using flowtable reduction and find the hazards in circuits	Applying (K3)
CO4	simplify the Boolean function and implement using Programmable logic array, essential cube theorem and compact algorithm	Applying (K3)
CO5	design the synchronous sequential circuits using Programmable Logic Device, Programmable Array Logic and CPLD	Applying (K3)

Mapping of COs with POs and PSOs

COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	3	3	2		3	3
CO2	3	3	2		2	3
CO3	3	3	2		3	3
CO4	3	3	2		3	3
CO5	3	3	2		3	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN – THEORY

Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	5	15	80				100
CAT2	5	15	80				100
CAT3	5	15	80				
ESE	10	10	80				100

* ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)

22ESC11 - VERILOG HDL FOR EMBEDDED FPGA PROCESSOR							
Programme& Branch	**M.E.- Embedded Systems**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**1**	**PE**	**2**	**0**	**2**	**3**

Preamble	To impart knowledge on designing and verification of integrated circuits using Verilog HDL and system Verilog and to understand MOS transistor theory.

Unit – I	**Verilogconcepts:**	**6**
Introduction- Design flow- Design hierarchy- components of a simulation- Basic concepts- Data types- System tasks and compilerDirectives-Modules and ports-test bench- Gate level Modeling-Dataflow Modeling-Behavioural Modeling-Switch level modeling.		
Unit – II	**LogicSynthesiswithVerilogHDL:**	**6**
VerilogHDLSynthesis-Synthesis Design Flow-Verification of the gate level net list - Modeling for logic synthesis- Example ofcombinational circuit synthesis.		
Unit – III	**Introduction to System Verilog:**	**6**
Data types and procedural statements: Built-In Data Types- Fixed-Size Arrays- Dynamic Arrays- Queues- Associative Arrays - Array Methods - Choosing a Storage Type - Creating New Types with typedef- Creating User-Defined Structures- Type conversion- Enumerated Types- Task and Function Overview- Routine Arguments- Returning from a Routine.		
Unit – IV	**Connecting the Test bench and Design:**	**6**
Separating the Test bench and Design-The Interface Construct-Stimulus Timing-Interface Driving and Sampling-Connecting It All Together-Top-Level Scope-Program – Module Interactions-System Verilog Assertions-The Four-Port ATM Router - Directed Test for the LC3 Fetch Block		
Unit – V	**MOS Transistor and CMOS Inverter Characteristics:**	**6**
Review of fabrication process-CMOS n-well process & SOI process-Layout Design Rules-Review of MOS transistor Theory: Structure, Operation-MOSFET Current-Voltage Characteristics-Threshold Voltage-MOSFET Capacitances-CMOS Inverter DC Characteristics-switching characteristics-power dissipation.		

LIST OF EXPERIMENTS / EXERCISES:

1.	Modeling of combinational digital systems with test benches
2.	Modeling of sequential digital systems with test benches
3.	Modeling of CMOS gates and Boolean functions
4.	Modeling of FSM and Memory design with test benches
5.	Design and implementation of ALU, MAC using FPGA
6.	Mini project

Lecture:30, Practical:30, Total:60

REFERENCES:

1.	Samir Palnitkar, “Verilog HDL: A Guide to Digital Design and Synthesis”, Pearson Education New Delhi, 2019.
2.	Chris Spear, “System Verilog for Verification: A Guide to Learning the Test bench Language Features”, 2nd Edition, Springer, 2012.
3.	Neil H.E. Weste, Kamran Eshraghian Principles of CMOS VLSI Design, 3rd Edition, Pearson Education ASIA, 2007.

COURSE OUTCOMES: On completion of the course, the students will be able to		BT Mapped (Highest Level)
CO1	apply digital design concepts and simulate Verilog programs for the combinational, sequential and transistor level design.	Applying (K3) Precision (S3)
CO2	design and synthesize combinational and sequential circuits using Verilog programming	Applying (K3) Precision(S3)
CO3	understand the basic principles of verification process and System Verilog	Understanding(K2)
CO4	Interface testbench and design environment	Applying (K3)
CO5	comprehend the principles of MOS Transistor theory, it's fabrication and MOS inverter structures with various parameters.	Understanding(K2)

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	3	3	2	3
CO2	3	3	3	3	2	3
CO3	3		3	3	2	3
CO4	3		3	3	2	3
CO5	3		3	3	2	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1	10	20	70				100
CAT2	10	55	35				100
CAT3	10	55	35				100
ESE	10	40	50				100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

22EST11 - MICROCONTROLLER SYSTEM DESIGN							
Programme& Branch	**ME &EMBEDDED SYSTEMS**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**1**	**PC**	**3**	**0**	**0**	**3**
Preamble	To learn assembly and C programmingfor8051,PIC18Fxxx microcontroller architecture andbe able to interface sensors and motors for project development.						
Unit – I	**8051 Architecture:**						**9**
Architecture - memory organization - addressing modes - instruction set - timers –counters- Interrupts -I/O ports – Serial Communication – Simple assembly language programming							
Unit – II	**8051 Programming:**						**9**
Timer Counter Programming - Serial Communication Programming - Interrupt Programming -Interfacing I/O Devices-RTOS for 8051– FullRTOS - Task creation and Run - LCD digital clock/thermometer usingFullRTOS							
Unit – III	**PIC Microcontroller:**						**9**
Architecture of PIC18FXX - memory organization - addressing modes - instruction set - I/O Port-Simple Assembly LanguageProgramming							
Unit – IV	**PIC MicrocontrollerPeripherals&Embedded C Programming:**						**9**
Introduction to Embedded C - I/O Port-Timers - I2C bus-A/D converter-UART-CCP modules -Interrupts -EEPROM memories							
Unit – V	**Hardware interfacing**						**9**
LCD Display -touch screen- Keypad - SPI Bus Protocol -DS1307 RTC- DC Motor Direction and Speed control using PWM –StepperMotor							
							Total:45

REFERENCES:

1.	Muhammad Ali Mazidi, Janice G. Mazidi and Rolin D McKinlay, The 8051 Microcontroller and Embedded Systems, 2nd edition,Prentice Hall, 2014.
2.	Muhammad Ali Mazidi, Rolin D McKinlay, Danny Causy, PIC Microcontroller and Embedded Systems using Assembly and Embedded C for PIC18, 2nd edition, Pearson Education, 2021.
3.	John Jovine, PIC Microcontroller Project Book, 2nd edition, McGraw Hill, New Delhi, 2004
4.	E-Resources:https://archive.nptel.ac.in/courses/117/104/117104072/

COURSE OUTCOMES: **On completion of the course, the students will be able to**		**BT Mapped (Highest Level)**
CO1	comprehend the architecture of 8051 and write assembly language program for arithmetic and logical operations	Understanding (K2)
CO2	write assembly language program for internal peripherals of 8051 microcontroller and demonstrate the concepts of RTOS for 8051 microcontrollers	Applying (K3)
CO3	comprehend the architecture of PIC18fxx and write assembly language program	Understanding (K2)
CO4	write ASM/ Embedded C programs to manipulate the peripherals of PIC18Fxx	Applying (K3)
CO5	demonstrate simple embedded applications using DS1307 RTC/DC Motor/Stepper Motor and other I/O devices	Applying (K3)

Mapping of COs with POs and PSOs

COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	1	2	3	2		
CO2	1	2	3	3		1
CO3	2		3	3		2
CO4	1	3	3	3	2	
CO5	3	3	2	3	2	2

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	5	15	80				100
CAT2	5	15	80				100
CAT3	5	15	80				100
ESE	10	10	80				100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

22EST12 - PROGRAMMING LANGUAGES FOR EMBEDDED SYSTEMS							
Programme& Branch	**ME &EMBEDDED SYSTEMS**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**1**	**PC**	**3**	**0**	**0**	**3**
Preamble	Toknowabouttheprogrammingtechniquesinvolvedinembeddedsystemdesignandtoimplement C, C++ and Python programs.						
Unit – I	**Embedded C Basics:**						**9**
Overview of C vs Embedded C – Constants - CPU registers as variables- Modified Data types- Operators and Expressions-Managing Input and Output Operations - Decision Making - Branching – Looping - Arrays							
Unit – II	**Embedded C Programming:**						**9**
User defined Functions - Structures and Unions –Pointers – File Management in C - Dynamic memory allocation and Linked Lists - Preprocessor							
Unit – III	**C++ Programming:**						**9**
Basics of C++ Programming - Namespace - objects and classes - working with classes - dynamic memory allocation - Inheritance - Reusing code in C++ - Friend functions - Exceptions - Input and Output operations –File Managements							
Unit – IV	**Python Fundamentals:**						**9**
Basics of Python Programming - Decision control statements - Functions and Modules - Python Strings - File handling - Classes and objects - Error and Exception handling							
Unit – V	**Application using Python Packages:**						**9**
Numpy- Intrinsic Array creation - replicating- joining/mutating existing array - pandas- matplotlib- Basicmatplotlib plots - Logarithmic plots - Scatter plots							
							Total:45

REFERENCES:

1.	Brain W.Kernighan, Dennis Ritche, “The C Programming Language”, 2nd Edition, Pearson, 2015.
2.	ReemaThareja, "Python Programming using problem solving approach", 1st Edition, Oxford Publication, 2017.
3.	Stanley B. Lippman, JoseeLajoie, Barbara E. Moo, "C++ Primer", 5th Edition, Pearson Education, 2013.
4.	A J Henley, Dave Wolf, "Learn Data Analysis with Python" ,Apress, 2018

COURSE OUTCOMES: **On completion of the course, the students will be able to**		**BT Mapped (Highest Level)**
CO1	write programs for data manipulation, I/O process, array and numerical conversions usingEmbedded C	Applying(K3)
CO2	apply advanced data structures for problem solving	Applying(K3)
CO3	apply object-oriented programming concepts for data manipulation	Applying(K3)
CO4	write python programs for data manipulations with object oriented and exception handling features	Applying(K3)
CO5	apply transformation, visualization and manipulation techniqueson data using python packages	Applying(K3)

Mapping of COs with POs and PSOs

COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	3	2	2	3	1	1
CO2	3	2	3	3	2	1
CO3	3	2	2	2	2	1
CO4	3	2	3	2	2	1
CO5	3	1	3	2		1

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	10	40	50				100
CAT2	10	50	40				100
CAT3	10	40	50				100
ESE	10	45	45				100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

22ESL11 - MICROCONTROLLER SYSTEM DESIGN LABORATORY							
Programme& Branch	**ME &EMBEDDED SYSTEMS**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**1**	**PC**	**0**	**0**	**2**	**1**

Preamble	To impart the knowledge of design and development of embedded applications using Microcontrollers

LIST OF EXPERIMENTS / EXERCISES/Projects:

1.	Introduction to Electronic system design • Explore the knowledge of Basic components, Switch, transformer, rectifier, and soldering • Design of simple voltage regulator • Design a simple circuit of Brightness control
2.	Room Automation Systemusing 8051 • To count Number of persons present in the hall • To control fan and light based on the number of persons • Design a simple circuit of Brightness control of light
3.	Controlling AC/DC appliances using Bluetooth (8051) • To design relay Controlled AC appliances like bulb ,Fan (12V DC motor)
4.	Overhead Tank water level indicator system with alarm and Auto-shutoff (PIC18F series) • To sense 5 level of indication o Full o High o Medium o Low o Very low
5.	Density based Traffic Control System(PIC18FXX series) • To control 4 way traffic signal • To use indicators and Sensor • To measure the density of each road and Display in LCD
6.	Automatic college bell management system(PIC18FXX series) • To use RTC to make precise and Accurate timing • To use keypad for timing adjustment • To use seven segment display for display timing information • To use buzzer or Electric Gong Bell to ring alarm
	Total:30

REFERENCES/ MANUAL /SOFTWARE:

1.	Laboratory Manual
2.	Proteus Professional/CCS Compiler/UMPS/MPLAB suite.

COURSE OUTCOMES: **On completion of the course, the students will be able to**		**BT Mapped (Highest Level)**
CO1	Program the I/O and timer modules of an 8-bit microcontroller for a counting application	Applying(K3), Precision(S3)
CO2	Write embedded C program for ADC, Serial communication and sensor interfacing using Proteus simulator	Applying(K3), Precision (S3)
CO3	Design and develop embedded based projects.	Applying(K3), Precision(S3)

Mapping of COs with POs and PSOs

COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	1		3	3	1	
CO2	2	2	3	3	3	
CO3	3	2	3	3	3	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

22ESL12 - PROGRAMMING LANGUAGES FOR EMBEDDED SYSTEMS LABORATORY							
Programme& Branch	**ME &EMBEDDED SYSTEMS**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**1**	**PC**	**0**	**0**	**2**	**1**

Preamble	To write program for various applications using C, C++ and Python.

LIST OF EXPERIMENTS / EXERCISES:	
1.	Multi-dimensional arrays handling by passing with /without argument to the user defined functions as pointer or array in C
2.	Implementation of singly/doubly linked list and its operations in C
3.	2D/n'D vector related operations using user defined datatype and save 2D/n'D feature vectors and resultant of vector operation in file using file management operations in CPP
4.	2D vector related operations as operator overloading of user-defined class in CPP
5.	User-defined class of Data Frame with its member functions of statistic operations with exception handling using python script
6.	Data manipulation, visualization and plotting charts using numpy, pandas and matplotlib packages respectively using python
	Total:30

REFERENCES/ MANUAL /SOFTWARE:	
1.	C/C++ interpreter
2.	Python 3 interpreter for Windows/Linux

COURSE OUTCOMES: **On completion of the course, the students will be able to**		**BT Mapped (Highest Level)**
CO1	represent the data as vectors and perform vector operations using C and C++ program	Applying(K3), Precision(S3)
CO2	construct linked list of data and perform linked list operations using C program	Applying (K3), Precision (S3)
CO3	handle big data frame work and perform statistic operations using python	Applying(K3), Precision(S3)

Mapping of Cos with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2		3	3	2	
CO2	3	3	3	3	2	
CO3	1	2	3	3	1	

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

22EST21 - EMBEDDED NETWORKING AND BUSES							
Programme& Branch	**ME &EMBEDDED SYSTEMS**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**2**	**PC**	**3**	**0**	**0**	**3**
Preamble	To understand the concepts of networking for embedded applications with respect to ISO/OSI standards.						
Unit – I	**Introduction to Networks:**						**9**
Introduction to Networks-Advantages and Disadvantages. OSI Model-Foundations of OSI Model. Protocol Standards. Grounding, Shielding &Noise							
Unit – II	**Embedded Communication:**						**9**
Introduction Serial/Parallel Communication Serial communication protocols: -RS232 standard RS485 Synchronous Serial Protocols -Serial Peripheral Interface (SPI) Inter Integrated Circuits (I2C) PC Parallel port programming -ISA/PCI Bus protocols							
Unit – III	**USB Protocol:**						**9**
Firewire- USB bus Introduction- Speed - Identification on the bus USB States USB bus communication: Packets Data flow types Enumeration Descriptors							
Unit – IV	**Ethernet Standards:**						**9**
Introduction-IEEE Standards-Ethernet MAC layer-IEEE 802.2 and Ethernet SNAP- OSI and IEEE 802.3 standard. Ethernet transceivers, Ethernet types, switches & switching hubs, 10 Mbps Ethernet, 100 Mbps Ethernet, Gigabit Ethernet. TCP / IP Overview- Internet Layer Protocols-Host-to-Host layer							
Unit – V	**Devicenet:**						**9**
Overview Layers Profibus-Overview-Protocol Stack. HART Protocol Overview- Layers. Foundation Field Bus- Layers-ErrorDetection and Diagnostics. CANBus Introduction - Frames Bit stuffing Types of errors Nominal Bit TimingPIC18Fxx microcontroller CAN Interface							
							Total:45

REFERENCES:

1. Steve Mackay. Edwin Wright, Deon Reynders, John Park, Practical Industrial data Networks: Design, Installation and Trouble Shooting, 1st Edition, Newnes publications-Elsevier 2004.
2. Dogan Ibrahim. Advanced PIC microcontroller projects in C, 2nd Edition Newnes publications-Elsevier 2014.
3. Jan Axelson. Parallel Port Complete: Programming, Interfacing& using the PC's Parallel port, 1st Edition, Lakeview Research Publications 1997.

COURSE OUTCOMES: **On completion of the course, the students will be able to**		**BT Mapped (Highest Level)**
CO1	realize the embedded communication with respect OSI model and its standards.	Understanding (K2)
CO2	illustrate the concepts of serial and parallel communication and its standards	Understanding (K2)
CO3	develop a system to transfer data between peripheral device and microcontroller through USB Protocol Understand the concepts of USB protocol	Understanding (K2)
CO4	analyze the different IEEE Standards, challenges and its solutions in wireless networks.	Applying(K3)
CO5	design bit stuffing and error detection and correction mechanisms for data at the sending and receiving end	Applying(K3)

Mapping of COs with POs and PSOs

COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	3	3	3	2	1	3
CO2	3	2	3	3		
CO3	3	3	2	2	3	
CO4	3	2	1	1		2
CO5	2	1			2	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	30	70					100
CAT2	30	70					100
CAT3	20	40	40				100
ESE	10	60	30				100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

22EST22 - SINGLE BOARD COMPUTER							
Programme& Branch	**ME &EMBEDDED SYSTEMS**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**2**	**PC**	**3**	**0**	**0**	**3**
Preamble	To develop a basic knowledge of working with single board computer for multifunctional tasks like IoT, Image analysis for research applications						
Unit – I	**Introduction to SBC and Linux Basics:**						**9**
Types of single board computer - Linux file system - text editors - accessing files - power supply unit - preparation of boot SD card - configuration - networking with Host computer - terminal access							
Unit – II	**Python Programming and Sensor Interfacing:**						**9**
Pin diagram - GPIO access - LED & Switch - Timers - external circuit interfacing - UART - sensor interfacing.							
Unit – III	**Peripheral Control:**						**9**
Interfacing touch screen - ADC, DAC and, Motor - DC Motor Control using PWM Relay and Stepper Motor interfacing.							
Unit – IV	**Internet of Things:**						**9**
Open API's for Internet of Things - collect and store sensor data - analyze and visualize data - control peripheral device.							
Unit – V	**Image Processing in SBC:**						**9**
Introduction to OPENCV - reading and writing images - create image - draw - conversion - merge - video processing - real-time image processing in SBC.							
							Total:45

REFERENCES:

1. Simon Monk, “Raspberry Pi Cookbook: Software and Hardware Problems and Solutions”, 3rd Edition, O’Reilly Media Inc, California, USA, 2020.
2. Guillermo Guillen, “Sensor Projects with Raspberry Pi: Internet of Things and Digital Image Processing”, A Press Media,1st Edition 2019.
3. Joe Minichino, Joseph Howse, “Learning OpenCV 4 Computer Vision with Python 3” Get to grips with tools, techniques, and algorithms for computer vision and machine learning", Third Edition, Packt Publishing Ltd., 2020, ISBN 978-1-78953-161-9.

COURSE OUTCOMES: **On completion of the course, the students will be able to**		**BT Mapped (Highest Level)**
CO1	describe the fundamentals of an SBC for development of embedded applications	Understanding (K2)
CO2	write program to access ports and interface peripherals	Applying (K3)
CO3	develop embedded applications using a single board computer	Applying (K3)
CO4	implement the concepts of internet of things in an SBC	Applying (K3)
CO5	apply image processing techniques in an SBC for real time applications	Applying (K3)

Mapping of COs with POs and PSOs

COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	3					
CO2	3	3	3			
CO3	2	2	3	2	3	2
CO4	2	2	3	2	3	2
CO5	2	2	3	2	3	2

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	10	30	60				100
CAT2	10	30	60				100
CAT3	10	30	60				100
ESE	10	35	55				100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

22ESC21 - EMBEDDED LINUX							
Programme& Branch	**M.E.- Embedded Systems**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**2**	**PC**	**3**	**0**	**2**	**4**

Preamble	To develop the embedded RTOS for any target board and to port the RTOS with necessary file system to the target board along with the bootloader.	
Unit – I	**Fundamentals of Linux:**	**9**
Basic Linux System Concepts: Working with Files and Directories - Introduction to Linux File system - Basic Linux commands and concepts Logging in - Shells - Basic text editing - Advanced shells and shell scripting - Processes and threads in Linux - Inter process communication -Linux System calls.		
Unit – II	**Various Distributions and Cross Platform Tool Chain:**	**9**
Introduction - History of Embedded Linux - Embedded Linux versus Desktop Linux - Embedded Linux Distributions - Architecture of Embedded Linux - Linux kernel architecture - User space Linux startup sequence - GNU cross platform Tool chain		
Unit – III	**Host-Target Setup and Overall Architecture:**	**9**
Real Life Embedded Linux Systems -Design and Implementation Methodology - Types of Host/Target Development Setups -Generic Architecture of an Embedded Linux System - System Startup - Types of Boot Configurations System Memory		
Unit – IV	**Kernel Configuration and Root File System:**	**9**
Selecting a Kernel - Configuring the Kernel - Compiling the Kernel - Installing the Kernel - Basic Root File System Structure - Libraries - Kernel Modules and Kernel Images -Setting Up the Bootloader U-boot		
Unit – V	**Embedded Storage and Driver:**	**9**
Memory Technology Device (MTD) MTD Architecture - MTD Driver for NOR Flash The Flash Mapping drivers MTD Block and character devices mtdutils package Embedded File Systems Optimizing storage space-Porting Roadmap Linux serial driver and Ethernet driver		

LIST OF EXPERIMENTS / EXERCISES:

1.	Linux file access
2.	Linux shell scripting
3.	Installation of Embedded Linux distribution
4.	Installation of tool chain for the specified target board
5.	Target Development setup and Boot Configurations
6.	Compiling a kernel, Building a kernel for specified target Board
7.	Configuring kernel modules, Images for specified target Board
8.	Loading the images in Flash memory

Lecture:45, Practical:30, Total:75

REFERENCES/ MANUAL / SOFTWARE:

1.	Karim Yaghmour. Jos Masters, Phillipe Gerum, Building Embedded Linux Systems, 2nd Edition, O'Reilly Publications, 2008
2.	P.Raghavan ,Amol Lad, Sriram Neelakandan. Embedded Linux System Design and Development, Auerbach Publications, New York, 2005.
3.	Paul Cobbaut. Linux Fundamentals, GNU Free Documentation License 2013

COURSE OUTCOMES: **On completion of the course, the students will be able to**		**BT Mapped (Highest Level)**
CO1	execute the fundamentals commands of linux OS and scripts	Applying(K3), Precision(S3)
CO2	demonstrate communication between kernel space and user space	Applying(K3), Precision(S3)
CO3	develop kernel images for embedded hardware	Applying (K3), Precision(S3)
CO4	develop system configuration and boot process	Applying (K3) , Precision(S3)
CO5	develop the bootloader and configuring the environmental variables for boot process to load the developed kernel images either in RAM or flash.	Applying (K3), Precision(S3)

Mapping of COs with POs and PSOs

COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	2	1				
CO2	3	2	2	1		
CO3	3	2	2	1		
CO4	3	2	2	2		
CO5	3	2	2	2		

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	30	30	40				100
CAT2	20	40	40				100
CAT3	20	35	45				100
ESE	10	40	50				100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

22ESL21 - SINGLE BOARD COMPUTER LABORATORY							
Programme& Branch	**ME &EMBEDDED SYSTEMS**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**2**	**PC**	**0**	**0**	**2**	**1**

Preamble	To develop real-time applications based on single board computer (SBC).

LIST OF EXPERIMENTS / EXERCISES:

1.	Interfacing a camera with SBC
2.	Design of metal detector using SBC
3.	Implement a face detection using SBC
4.	Implementation of attendance monitoring system with student identity card using SBC
5.	Design of an IoT based weather monitoring device using SBC
6.	Design of burglar detector with photo capture using SBC

Total:30

REFERENCES/ MANUAL /SOFTWARE:

1.	Santos, Rui, and Sara Santos. 20 Easy Raspberry Pi Projects: Toys, Tools, Gadgets, and More!. No Starch Press, 2018.
2.	Python 3 documentation

COURSE OUTCOMES: **On completion of the course, the students will be able to**		**BT Mapped (Highest Level)**
CO1	write programs to interface various peripherals with SBC	Applying(K3), Precision(S3)
CO2	develop embedded and IoT applications using SBC	Applying (K3), Precision (S3)
CO3	implement computer vision and image processing using SBC	Applying (K3), Precision(S3)

Mapping of Cos with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2		3	3	2	
CO2	3	3	3	3	2	
CO3	1	2	3	3	1	

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

22ESL22 - EMBEDDED NETWORKING AND BUSES LABORATORY							
Programme& Branch	**ME &EMBEDDED SYSTEMS**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**2**	**PC**	**0**	**0**	**2**	**1**

Preamble	To impart knowledge of design and development of embedded products

LIST OF EXPERIMENTS / EXERCISES:

1.	Simulation of Serial port programming using RS232
2.	Subnetting using IPV4
3.	TCP simulation using Netsim
4.	UDP simulation using Netsim
5.	Realization of Address Resolution Protocol
6.	Design a client server model and simulate and analysis of real packet transmission in a network using NS3.
7.	Design and analysis of TCP/IP packet using network protocol analyzer
8.	Realisation of TP for Bulk transfer using Protocol analyzer

Total:30

REFERENCES/ MANUAL /SOFTWARE:

1.	Netsim
2.	Proteus

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	develop serial port programming using RS standards.	Applying(K3), Precision(S3)
CO2	design and develop subnetting for an organization for various departments.	Applying(K3), Precision(S3)
CO3	design and develop networking model using TCP and UDP	Applying(K3), Precision(S3)

Mapping of Cos with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	2	3		2	
CO2	3	3	3		2	3
CO3	3	2			3	2

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

22ESP31 - PROJECT WORK - I							
Programme& Branch	**ME &EMBEDDED SYSTEMS**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**3**	**EC**	**0**	**0**	**16**	**8**

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	formulate a problem statement for the problem given by the industry.	Applying (K3)
CO2	summarize the literature review	Understanding (K2)
CO3	develop a methodology for the identified problem	Applying (K3
CO4	carry out the experimental work and analyse the performance as per the specified methodology in VLSI domain.	Analyzing (K4)
CO5	prepare and present the project report	Applying (K3)

Mapping of Cos with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	2	3	3	2	3
CO2	2	3	2	2	2	3
CO3	3	2	3	3	3	3
CO4	3	3	3	3	3	3
CO5	2	3	2	2	3	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

22ESP31 - PROJECT WORK - II							
Programme& Branch	**ME &EMBEDDED SYSTEMS**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**4**	**EC**	**0**	**0**	**12**	**24**

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	identify the problem and formulate a problem statement	Applying (K3)
CO2	summarize the literature review	Understanding (K2)
CO3	develop a suitable innovative methodology	Applying (K3
CO4	carry out the experimental work and analyse the performance as per the specified innovative methodology in VLSI domain.	Analyzing (K4)
CO5	prepare and present the project report	Applying (K3)

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	2	3	3	2	3
CO2	2	3	2	2	2	3
CO3	3	2	3	3	3	3
CO4	3	3	3	3	3	3
CO5	2	3	2	2	3	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

22VLE01 - TESTING OF VLSI CIRCUITS (Common to VLSI Design and Embedded Systems branches)							
Programme& Branch	**ME - VLSI DESIGN & ME - EMBEDDED SYSTEMS**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**2**	**PE**	**3**	**0**	**0**	**3**
Preamble	To know the basics of VLSI test concepts, test generation, DFT architectures, Built in SelfTest, memory testing and test compression.						
Unit – I	**Fault modeling and simulation:**						**9**
Importance of Testing- Challenges in VLSI Testing -Fault models- Logic simulation- Compiled code simulation-Event driven simulation- Fault simulation- Serial fault simulation- Parallel fault simulation- Deductive fault simulation- Concurrent fault simulation							
Unit – II	**Design For Testability:**						**9**
Testability analysis –DFT basics- Scan cell designs- Scan architectures- Scan design rules- Scan design flow							
Unit – III	**Test Generation:**						**9**
Random test generation- Designing a stuck-at model- ATPG for Combinational Circuits- Designing a sequential ATPG- Designing Simulation based ATPG-Hybrid deterministic and simulation based ATPG.							
Unit – IV	**Built In Self Test:**						**9**
BIST design rules- Test pattern generation- Output response analysis- Logic BIST architectures							
Unit – V	**Test compression and Memory Testing:**						**9**
Test stimulus compression- Code based schemes - RAM functional fault models – Dynamic faults- Functional test patterns and algorithms-March tests-Word-oriented memory- Multi-port memory.							
							Total:45

REFERENCES:

1.	Laung – Terngwang, Cheng – wen wu, Xidogingwen, “VLSI Testing Principles and Architectures: Design for Testability”, Morgan Kaufmann Publisher, 2011.
2.	Abramovici, M., Breuer, M.A and Friedman, A.D., “Digital Systems and Testable Design”, Jaico Publishing House, 2014.
3.	Bushnell, M.L and. Agrawal, V.D., “Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits”, Kluwar Academic Publishers, 2002.

COURSE OUTCOMES: On completion of the course, the students will be able to		BT Mapped (Highest Level)
CO1	distinguish between different fault models and types of simulation	Understanding (K2)
CO2	identify the design for testability techniques for combinational and sequential circuits	Understanding (K2)
CO3	apply various test generation methods for combinational and sequential circuits	Applying (K3)
CO4	compare the various Built In Self Test architectures	Understanding (K2)
CO5	understand the various fault models for memory, test generation algorithms for memories and test compression approaches	Understanding (K2)

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		3	2	3	3
CO2	3		3	2	3	3
CO3	3		3	2	3	3
CO4	3		3	2	3	3
CO5	3		3	2	3	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN – THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1	15	85					100
CAT2	15	55	30				100
CAT3	15	85					100
ESE	5	80	15				100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

22ESE01 - DISTRIBUTED EMBEDDED COMPUTING							
Programme& Branch	**ME &EMBEDDED SYSTEMS**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**2**	**PE**	**3**	**0**	**0**	**3**

Preamble	This course enables the students to understand the concept of distributed computing infrastructure, concept of Internet and programming language used.	
Unit – I	**The Hardware Infrastructure:**	**9**
Broadband Transmission facilities – Open Interconnection standards – Local Area Networks – Wide Area Networks – Network management – Network Security – Cluster computers.		
Unit – II	**The Internet Concepts:**	**9**
Capabilities and limitations of the Internet – Interfacing Internet server applications to corporate databases HTML and XML Web page design and the use of active components.		
Unit – III	**Distributed Computing using JAVA:**	**9**
IO streaming – Object serialization – Networking – Threading – RMI – multicasting – distributed databases – embedded java concepts – case studies.		
Unit – IV	**Embedded Agent:**	**9**
Introduction to the embedded agents – Embedded agent design criteria – Behavior based, Functionality based embedded agents – Agent co-ordination mechanisms and benchmarks embedded-agent. Case study: Mobile robots.		
Unit – V	**Embedded Computing Architecture:**	**9**
Synthesis of the information technologies of distributed embedded systems – analog/digital codesign – optimizing functional distribution in complex system design – validation and fast prototyping of multiprocessor system-on-chip – a new dynamic scheduling algorithm for real-time multiprocessor systems.		
		Total:45

REFERENCES:

1.	Bernd KleinjohannClab, Architecture and Design of Distributed Embedded Systems, 1st Edition, Kluwer Academic Publisher, Boston, April 2001.
2.	George Coulouris and Jean Dollimore, Distributed Systems – concepts and design,5th Edition, Addison – Wesley 2012.
3.	Sape Mullender, Distributed Systems, 2ndEdition, Addison-Wesley, 1993.

COURSE OUTCOMES: On completion of the course, the students will be able to		BT Mapped (Highest Level)
CO1	understand about the Hardware Infrastructure	Understanding(K2)
CO2	know the concept of Internet for computing applications	Applying(K3)
CO3	use the concept of JAVA in Distributed Embedded Computing	Applying(K3)
CO4	determine the role of embedded agent for simple applications	Applying(K3)
CO5	know the usage of embedded computing architectures	Understanding(K2)

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		3			
CO2	3		3	3		
CO3	3	1	3		2	
CO4	3	2	3	3	2	1
CO5	3	2	3	3	2	1

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1	10	60	30				100
CAT2	-	40	60				100
CAT3	10	50	40				100
ESE	10	50	40				100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

22ESE02 - SOLAR AND ENERGY STORAGE SYSTEM							
Programme& Branch	**ME &EMBEDDED SYSTEMS**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**2**	**PE**	**3**	**0**	**0**	**3**
Preamble	To understand and apply the process of PV systems, power point tracking and design of PV systems.						
Unit – I	**Introduction to Solar Cells:**						**9**
Characteristics of sunlight – semiconductors and P-N junctions –behavior of solar cells – cell properties – PV cell interconnection							
Unit – II	**Stand Alone PV System:**						**9**
Schematics, Components, Batteries, Charge Conditioners-Balance of system components for DC and/or AC Applications-Typical applications for lighting, water pumping etc.							
Unit – III	**Grid Connected PV Systems:**						**9**
Schematics, Components, Charge Conditioners, Interface Components-Balance of system Components -PV System in Buildings.							
Unit – IV	**Maximum Power Point Tracking:**						**9**
MPPT concept, Input impedance of DC-DC converters -Boost converter, Buck converter, Buck-Boost converter, PV module in SPICE, Simulation - PV and DC-DC interface-MPPT ALGORITHMS**-**Impedance control methods, Reference cell, Sampling method, Power slope methods, Hill climbing method, Practical points - housekeeping power supply, Gate driver, MPPT for non-resistive loads, Simulation.							
Unit – V	**Design of PV Systems:**						**9**
Radiation and load data-Design of System Components for different PV Applications-Sizing and Reliability-Simple Case Studies: Solar Lighting-Solar Cooking-Solar Drying-Solar Desalination-Solar Furnaces.							
							Total:45

REFERENCES:

1.	Chetan Singh Solanki, Solar Photovotaics–Fundamentals, Technologies and Applications, 3rd Edition, PHI Learning Pvt. Ltd., 2015.
2.	Nayak J.K, Sukhatme S. P., Solar Energy, 4th Edition, Tata McGraw Hill, 2018
3.	Chenming, Hu. And Richard M.White, Solar Cells from Basic to Advanced Systems, McGraw Hill Book Co, 1983.

COURSE OUTCOMES: **On completion of the course, the students will be able to**		**BT Mapped (Highest Level)**
CO1	infer the characteristics of sunlight and the role of semiconductors in solar cell	Understanding (K2)
CO2	relate types and design of various PV - interconnected systems.	Applying(K3)
CO3	experiment with grid connected PV systems	Applying(K3)
CO4	apply the concepts of MPPT algorithm for PV modules	Applying(K3)
CO5	design PV systems for different applications	Applying(K3)

Mapping of COs with POs and PSOs

COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1			3	2		
CO2			3	2		
CO3	2		3	2		
CO4	1		3	2		
CO5	3		2	3		2

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	10	40	50				100
CAT2	10	40	50				100
CAT3	10	50	40				100
ESE	10	40	50				100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

22ESF01 - ASIC FOR EMBEDDED SYSTEMS							
Programme& Branch	**M.E-EMBEDDED SYSTEM**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Verilog HDL for Embedded FPGA Processor**	**2**	**PE**	**2**	**0**	**2**	**3**

Preamble	To know the different programmable ASICs, logic cells, I/O cells and interconnect and to learn how synthesis and physical design flow in carried out in an ASIC design.	
Unit – I	**Introduction to ASICs, CMOS Logic and ASIC Library Design:**	**6**
Types of ASICs - Design flow - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort.		
Unit – II	**Programmable ASICs, Programmable ASIC Logic Cells and Programmable ASIC I/O Cells:**	**6**
Anti fuse - static RAM - EPROM and EEPROM technology - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.		
Unit – III	**Programmable ASIC Interconnect:**	**6**
Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX9000 - Altera FLEX.		
Unit – IV	**Design and synthesis:**	**6**
Design systems - Half gate ASIC –Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation-.Logic synthesis – Logic Simulation - Design and synthesis of various circuits.		
Unit – V	**Physical Design:**	**6**
ASIC Partitioning - floor planning- placement and routing – power and clocking strategies - DRC.		

LIST OF EXPERIMENTS / EXERCISES:	
1.	Design, simulation and synthesis of Adders
2.	Design, simulation and synthesis of multipliers
3.	Design, simulation and synthesis of memory
	For the following the circuits, a) Perform the functional verification b) Synthesis the design c) Generate the layout (Automatic) d) Tabulate the area, power, delay
4.	8-bit microprocessor
5.	4-tap FIR Filter
6.	Miniproject

Lecture:30, Practical:30, Total:60

REFERENCES:

1.	Micheal John Sebastian Smith, Application - Specific Integrated Circuits, 12th compression, Pearson,2013
2.	Steve Kilts, “Advanced FPGA Design: Architecture, Implementation, and Optimization” Wiley Inter-Science, 2016
3.	Roger Woods, John McAllister, Gaye Lightbody, Dr. Ying Yi, FPGA-based Implementation of Signal Processing Systems, 2nd Edition, Wiley, 2017

COURSE OUTCOMES: On completion of the course, the students will be able to		BT Mapped (Highest Level)
CO1	understand ASIC Design flow and Design Libraries	Understanding(K2), Precision(S3)
CO2	understand the ASIC programming technology and programmable ASIC I/O cells	Understanding(K2), Precision(S3)
CO3	summarize the architecture of programmable ASIC interconnects	Understanding(K2), Precision(S3)
CO4	infer synthesis concept and perform physical design of digital circuits	Understanding(K2), Precision(S3)
CO5	apply the algorithms used in partitioning, floorplanning, placement, routing, power and clock design for ASIC and analyze the performance of digital systems using ASIC Design tool	Applying(K3), Precision(S3)

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	**3**		3	3	2	3
CO2	**3**		3	3	2	3
CO3	**3**		3	3	2	3
CO4	**3**	3	3	3	2	3
CO5	**3**	3	3	3	2	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1	20	60	20				100
CAT2	10	50	40				100
CAT3	10	40	50				100
ESE	10	40	50				100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

22ESE04 - QT CROSS COMPILING APPLICATION DEVELOPMENT							
Programme& Branch	**ME &EMBEDDED SYSTEMS**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**2**	**PE**	**3**	**0**	**0**	**3**
Preamble	To know the basic concepts of QT - single cross platform and to use C++ tool to design, develop, test, deploy programs for real time applications.						
Unit – I	**Introduction to C++:**						**9**
Basic Concepts - Conditionals and Loops - Data Types, Arrays, Pointers – Functions -Classes and Objects - Inheritance & Polymorphism – sample programs.							
Unit – II	**QT installation and compilation:**						**9**
Qt Basics– features - Qt Widgets - Learning the landscape – Build pro file - breakpoints – Examining variables and memory - Projects pane and building project - Example with Qt Widgets.							
Unit – III	**Qt Designer:**						**9**
Main form - application resources - Instantiating forms - message boxes - dialogs - Wiring the Qt Widgets application logic - declarative user interface development.							
Unit – IV	**QtIoT:**						**9**
Representing data using core classes - key-value pairs – Multithreading - Accessing files - Accessing HTTP resources - XML parsing with HTTP.							
Unit – V	**Application development:**						**9**
Managing widget layout – Model View Controller programming - Analyzing a concrete model subclass - MVC model on Qt Creator – sample applications development.							
							Total:45

REFERENCES:

1.	Lee Zhieng, Ray Rischpater, Application Development with Qt Creator, 3rd Edition, Packt Publishing Ltd, Birmingham, UK, 2020.
2.	Herbert Schildt, C++: The Complete Reference, 4th Edition, Osborne McGraw-Hill, U.S.A. 2017.

COURSE OUTCOMES: **On completion of the course, the students will be able to**		**BT Mapped (Highest Level)**
CO1	use class level C++ programs for simple applications.	Applying(K3)
CO2	apply the process of QT installation, compilation with simple application.	Applying(K3)
CO3	develop graphic user interface with application resources.	Applying(K3)
CO4	apply QT for Internet of things.	Applying(K3)
CO5	develop basic applications for different OS platform.	Applying(K3)

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1			3	2		
CO2			3	2		
CO3	2		3	2		1
CO4			3	1		
CO5	2		3	3	2	2

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1	10	90					100
CAT2	10	90					100
CAT3	10	50	40				100
ESE	10	70	20				100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

22ESE05 - SENSORS AND ACTUATORS FOR ROBOTICS							
Programme& Branch	**ME &EMBEDDED SYSTEMS**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**2**	**PE**	**3**	**0**	**0**	**3**
Preamble	To learn and infer the parameters components of robotics such as parallel and grippers , manipulators, sensors and actuators						
Unit – I	**Introduction to Robotics:**						**9**
Definition and origin of robotics – different types of robotics – various generations of robots – degrees of freedom – Asimovs laws of robotics – dynamic stabilization of robots.							
Unit – II	**Sensors and Actuators:**						**9**
Sensors: Machine vision – ranging – laser – acoustic– magnetic, fiber optic and tactile sensors. Actuators: Manipulator dynamics and force control – electronic and pneumatic manipulator control circuits – end effectors – various types of grippers – design considerations. Drives: Hydraulic, pneumatic and electric drives							
Unit – III	**Mechatronics:**						**9**
Determination of HP of motor and gearing ratio – variable speed arrangements – path determination Solution of inverse kinematics problem – multiple solution jacobian work envelope – hill Climbing Techniques.							
Unit – IV	**Robot Programming:**						**9**
Introduction to robot programming languages – classification of robot languages – Computer control and robot software – VAL system and Language							
Unit – V	**Applications of Robots:**						**9**
Multiple robots – machine interface – robots in manufacturing and non- manufacturing applications – robot cell design – selection of robot.							
							Total:45

REFERENCES:

1.	Deb. S.R. Robotics Technology and flexible Automation, 2nd Edition, McGraw Hill Publication, New Delhi, 2010.
2.	Nicholas Odrey, Mitchell Weiss, MikellGroover, Roger N.Nagel, Ashish Dutta, Industrial Robotics, 2nd Edition, McGraw-Hill Singapore, 2012.
3.	Ghosh, Control in Robotics and Automation: Sensor Based Integration, 1st Edition, Allied Publishers, Chennai, 1999.
4.	Richard D. Klafter, Thomas A. Chmielewski, Michael Negin, Robotic Engineering: An Integrated Approach, 1st Edition, Prentice Hall India, New Delhi, 2007.

COURSE OUTCOMES: **On completion of the course, the students will be able to**		**BT Mapped (Highest Level)**
CO1	infer the functions of a robot.	Understanding (K2)
CO2	interpret the type of sensors, actuators and drives for robots.	Understanding (K2)
CO3	apply the kinematics and path planning for robot applications.	Applying(K3)
CO4	experiment robot operations using VAL robot programming language.	Applying(K3)
CO5	apply the principles of robots for manufacturing Industries.	Applying(K3)

Mapping of COs with POs and PSOs

COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1			3	2		
CO2	1		3	2		
CO3	1		3	2		
CO4			3	2		
CO5	2		2	3	1	2

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	10	30	60				100
CAT2	10	30	60				100
CAT3	10	30	60				100
ESE	10	30	60				100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

22ESE06 - SIGNAL AND IMAGE PROCESSING FOR REAL TIME APPLICATIONS							
Programme& Branch	**ME &EMBEDDED SYSTEMS**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**2**	**PE**	**3**	**0**	**0**	**3**
Preamble	To develop the image processing tools from scratch, rather than using any image processing library functions						
Unit – I	**Digital Image Fundamentals:**						**9**
Elements of digital image processing systems- Brightness- Contrast- Hue- saturation- Mach band effect -2D Image sampling- 2D Image transforms: DCT – KLT – Haar. Image Enhancement: Basic intensity transformations – Histogram equalization - Spatial filtering: Smoothing and sharpening Filters – Frequency domain filtering : Smoothing and sharpening filters – Homomorphic filters							
Unit – II	**Morphological Image Processing:**						**9**
Erosion – Dilation – Duality – Opening – Closing – Hit or Miss Transformation– Basic Morphological Algorithms : Boundary Extraction- Hole filling – Extraction of connected components – Thinning – Thickening – Grayscale Morphology – Morphological smoothing – Morphological gradient – Tophat and bottom hat transformation							
Unit – III	**Image Segmentation:**						**9**
Point, line and edge detection – Basics of intensity thresholding – Region based segmentation: Region growing - Region splitting and merging. Image Compression: Fundamentals: Types of redundancy – Huffmann – Run length coding – Arithmetic coding - Block Transform coding							
Unit – IV	**Pattern recognition:**						**9**
Patterns and Pattern classes – Representation of Pattern classes – Approaches to object recognition :Baye's Parametric classification – Template matching method – Structural Pattern Recognition : statistical and structural approaches							
Unit – V	**Overview of speech processing:**						**9**
Speech Fundamentals: Articulatory Phonetics – Production and Classification of Speech Sounds; Acoustic Phonetics – acoustics of speech production; Short time Homomorphic Filtering of Speech; Linear Prediction (LP) analysis: Basis and development, LPC spectrum.							
							Total:45

REFERENCES:

1.	Gonzalez.R.C, Woods. R.E, Digital Image Processing, 4th Edition, Pearson Education, 2009
2.	Jayaraman.S, Esakkirajan.S, Veerakumar.T, Digital Image Processingll, 1st Edition Tata McGraw-Hill, New Delhi, , 2009.
3.	Hayes, Monson H. Statistical Digital Signal processing and Modeling, 1st Edition, John Wiley and Sons, Inc., 1996

COURSE OUTCOMES: On completion of the course, the students will be able to		BT Mapped (Highest Level)
CO1	interpret the basic image processing spatial domain characteristics of digital images	Understanding (K2)
CO2	apply Haar, DCT and KL Transforms to transform from spatial domain to other domains	Applying(K3)
CO3	apply morphological operators and segmentation algorithms to extract the edges and regions of interest and employ different coding techniques to compress the images	Applying(K3)
CO4	Apply the pattern recognition for the recognition of different class of objects	Applying(K3)
CO5	outline the speech processing approaches with homomorphic filtering of speech and linear prediction analysis	Applying(K3)

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1			3	3		
CO2			3	2		
CO3	2		3	3		
CO4	2		3	3		
CO5			2	3		

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1	20	80					100
CAT2	20	60	20				100
CAT3	10	30	60				100
ESE	10	45	45				100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

22VLE04 - LOW POWER VLSI DESIGN (Common to VLSI Design and Embedded Systems branches)							
Programme& Branch	**ME - VLSI DESIGN & ME - EMBEDDED SYSTEMS**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**VLSI Design Techniques**	**2**	**PE**	**3**	**0**	**0**	**3**

Preamble	To design a low power digital circuits and analyze the various power optimization methods	
Unit – I	**Sources of Power Dissipation and Power Optimization:**	**9**
Components of power dissipation in CMOS Circuits- Logic level power optimization- Problem formulation- Combinational circuits Technology independent optimization- Sequential circuits -Technology independent optimization- Technology-dependent optimization		
Unit – II	**Circuit Level Techniques for Low Power Design:**	**9**
Circuit level low-power design- Logic style- Latches and Flip-flops- Transistor sizing and ordering- Drivers for large load- Power, and Delay in CMOS circuits- CMOS circuit design styles for adders- Power delay and area comparisons for 4-bit RCA, adders and multipliers		
Unit – III	**Low Power System Design:**	**9**
Conventional arithmetic and low power design- Logarithmic Number System- Residue Number System- Reducing power consumption in memories- Static random access memories- Dynamic random access memories		
Unit – IV	**Low Power Clock Design and Power Estimation:**	**9**
Low-Power Clock Design- Interconnect Delays- Classification of power estimation methodologies- Simulation based power estimation- Probabilistic methods.		
Unit – V	**Software Design for Low Power:**	**9**
Sources of software power dissipation- Software power estimation- Software power optimization- Automated low power code generation- Co-design for low power.		
		Total:45

REFERENCES:

1.	Dimitrios Soudris, Chirstian Pignet, Costas Goutis, “Designing CMOS Circuits for Low Power”, Kluwer, 2002.
2.	Kaushik Roy and S.C.Prasad, “Low power CMOS VLSI circuit design”, Wiley, 2018.
3.	Ajit Pal, “Low-Power VLSI Circuits and Systems”, 1st Edition, Springer 2015.

COURSE OUTCOMES: **On completion of the course, the students will be able to**		**BT Mapped (Highest Level)**
CO1	enumerate the different sources of power dissipation in CMOS and various logic level power optimization techniques	Understanding (K2)
CO2	apply various power optimization techniques at circuit level.	Applying (K3)
CO3	design low power circuits at architecture level and memories	Applying (K3)
CO4	outline simulation and probabilistic method of power analysis and low power issues at low level design	Understanding (K2)
CO5	perform power estimation and optimization at programming level	Understanding (K2)

Mapping of COs with POs and PSOs

COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	3		3	3	3	3
CO2	3		3	3	3	3
CO3	3		3	3	3	3
CO4	3		3	3	3	3
CO5	3		3	3	3	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN – THEORY

Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	15	65	20				100
CAT2	15	35	50				100
CAT3	15	85					100
ESE	10	60	30				100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

22ESE07 - RTOS FOR EMBEDDED SYSTEM							
Programme& Branch	**ME &EMBEDDED SYSTEMS**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**2**	**PE**	**3**	**0**	**0**	**3**

Preamble	To provide a clear description of the concepts that underlie operating systems such as the ability to complete performance measurements at run-time, to direct the signal or send messages to tasks and to achieve pending on multiple kernel objects.	
Unit – I	**Introduction to Operating Systems:**	**9**
Function of OS –Computer system organization – Computer System Architecture - Operating system Operations – Process management – Memory Management – Protection and Security - System Structures: Operating system Services – User and Operating system Interface – System calls – Types of System Calls – Operating systems design and Implementation – Operating system Structure.		
Unit – II	**Real Time Systems:**	**9**
Overview-System Characteristics-Hard Real Time and Soft real time systems - Features of Real time kernels- - RTOS Concepts: Foreground/Background systems – Real time kernels – RTOS – Scheduling: Preemptive scheduling – Scheduling Points - Round robin scheduling – scheduling Internals		
Unit – III	**µC/OS-III:**	**9**
Introduction - µC/OS-III Features - Goals of µC/OS-III – Directories and Files – Critical Sections- Tasks –Task States – Task Scheduling – Idle Task – Statistics Task – Interrupts Under µC/OS-III – Clock Tick - µC/OS-III Initialization. Task Management: Assigning Task Priorities-Determining the size of stack-Detecting Task stack overflows-Task management services-Task Management Internals-Internal Tasks - Time Management.		
Unit – IV	**Resource Management:**	**9**
Disable/Enable Interrupts - Lock/Unlock- Semaphores- Mutex semaphore – Deadlock – Synchronization: Semaphore – Task Semaphore – Event Flags -Synchronizing multiple tasks. Message Passing: Messages – Messages Queues – Task Message Queue –Flow control – using message queues – clients and servers – message queue Internals.		
Unit – V	**Memory Management:**	**9**
Creating a memory Partition- getting a Memory Block from partition– Returning a Memory Block to a partition-using memory partitions- Porting µC/OS-III: µC/CPU-µC/OS-III Port- Board support Package - Case study of coding for an Automatic Chocolate Vending Machine using MUCOS RTOS.		
		Total:45

REFERENCES:

1.	A. Silberschatz, P. B. Galvin, G. Gagne, “Operating System Concepts”, 8th Edition, Wiley, 2009.
2.	Jean J. Labrosse. µC/OS - III The Real Time Kernel User’s Manual ,Micrium Press,.2009.
3.	Raj Kamal, "Embedded Systems: Architecture, Programming and Design", 2nd Edition, Tata Mcgraw Hill Education, 2011.

COURSE OUTCOMES: **On completion of the course, the students will be able to**		**BT Mapped (Highest Level)**
CO1	outline the characteristics of real time systems	Understanding(K2)
CO2	realize the concepts of scheduling employed in RTOS	Understanding(K2)
CO3	apply task creation, priority assignment, and time management services provided by µC/OS – III	Applying(K3)
CO4	apply semaphore, mutex, and message queue services in a task	Applying(K3)
CO5	demonstrate memory partitions and allocations techniques used in RTOS and identify the functions involved in porting µC/OS - III to a different architecture	Applying(K3)

Mapping of COs with POs and PSOs

COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1			3	2		
CO2			3	2		
CO3	2	2	3	2	2	
CO4	2	2	3	2	2	
CO5	2		3	2		3

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	10	50	40				100
CAT2	10	30	60				100
CAT3	10	30	60				100
ESE	10	30	60				100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

22ESE08 - MULTICORE PROCESSOR AND COMPUTING							
Programme& Branch	**ME &EMBEDDED SYSTEMS**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**3**	**PE**	**3**	**0**	**0**	**3**

Preamble	To know the basic knowledge about multiprocessor, multicomputer systems and advanced processor technology in parallel processors	
Unit – I	**MULTI-CORE PROCESSORS:**	**9**
Single core to Multi-core architectures – SIMD and MIMD systems – Interconnection networks - Symmetric and Distributed Shared Memory Architectures – Cache coherence - Performance Issues –Parallel program design.		
Unit – II	**PARALLEL PROGRAM CHALLENGES:**	**9**
Performance – Scalability – Synchronization and data sharing – Data races – Synchronization primitives (mutexes, locks, semaphores, barriers) – deadlocks and live locks – communication between threads (condition variables, signals, message queues and pipes).		
Unit – III	**SHARED MEMORY PROGRAMMING WITH OpenMP:**	**9**
OpenMP Execution Model – Memory Model – OpenMP Directives – Work - sharing Constructs - Library functions – Handling Data and Functional Parallelism – Handling Loops - Performance Considerations.		
Unit – IV	**DISTRIBUTED MEMORY PROGRAMMING WITH MPI:**	**9**
MPI program execution – MPI constructs – libraries – MPI send and receive – Point - to - point and Collective communication –MPI derived data types – Performance evaluation.		
Unit – V	**PARALLEL PROGRAM DEVELOPMENT:**	**9**
Case studies - n - Body solvers – Tree Search –OpenMP and MPI implementations and comparison.		
		Total:45

REFERENCES:

1.	Peter S. Pacheco, An Introduction to Parallel Programming, Morgan - Kauffman/Elsevier, 2011
2.	Darryl Gove, Multicore Application Programming for Windows, Linux, and Oracle Solaris, Pearson, 2011
3.	Michael J Quinn, Parallel programming in C with MPI and OpenMP, Tata McGraw Hill, 2017
4.	Jason Roberts ,Shameem Akhter, Multi-core Programming: Increasing Performance through Software Multi-threading, Intel Press, 2010

COURSE OUTCOMES: **On completion of the course, the students will be able to**		**BT Mapped (Highest Level)**
CO1	interpret the operations of multiprocessor and multicomputer systems.	Understanding(K2)
CO2	Know the advanced processor technology, pipelining and scalable architectures.	Understanding(K2)
CO3	develop programs using OpenMP.	Applying(K3)
CO4	write simple programs for distributed memory in MPI	Applying(K3)
CO5	develop programming for serial processors parallel processors.	Applying(K3)

Mapping of COs with POs and PSOs

COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1			3	3		
CO2			3	2		
CO3	2	2	3	2	2	1
CO4	2	2	2	3	2	1
CO5			3	3		2

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	10	90					100
CAT2	10	50	40				100
CAT3		50	50				100
ESE	10	50	40				100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

22ESE09 - VIRTUAL INSTRUMENTATION FOR INDUSTRIAL APPLICATIONS							
Programme& Branch	**ME &EMBEDDED SYSTEMS**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**3**	**PE**	**3**	**0**	**0**	**3**
Preamble	To impart knowledge about advanced tools in virtual instrumentation to develop new industrial applications.						
Unit – I	**Graphical Programming Environment:**						**9**
Introduction- History of Virtual Instrumentation- LabVIEW and VI- Conventional and Graphical Programming - Components of LabVIEW- Tools and Other Palettes- Arranging Objects- Pop-up menus- Color Coding- Code Debugging- Context Sensitive Help- Types of VIs- Creating Sub-VIs.							
Unit – II	**Introduction to LabVIEW:**						**9**
LabVIEW Environment - Front Panel - Block Diagram - Building GUI - Loops - Execution Structures – Data types.							
Unit – III	**LabVIEW Programming:**						**9**
Arrays - Clusters - Charts - Graphs - Structures - String and File I/O- Data Flow Programming.							
Unit – IV	**Data Acquisition:**						**9**
Instrument Control - GPIB - VISA - Instrument Drivers - DAQ Basics - Signal Conditioning - DAQ Hardware - Analog I/O and Digital I/O - DAQ Assistant - Components of Computer Based Measurement System.							
Unit – V	**Embedded Programming with LabVIEW:**						**9**
CompactRIO - Setting Up CompactRIO system - Implementing an Embedded Program - Accessing I/O - Interfacing FPGA and Real time processor - Embedded State Machine - Case Study: Temperature Monitor using myRIO.							
							Total:45

REFERENCES:

1.	Jovitha Jerome. Virtual Instrumentation using LabVIEW, 3rd Edition, PHI Learning Pvt. Ltd, New Delhi, 2012
2.	Jeffrey Travis, Jim Kring. LabVIEW for Everyone: Graphical Programming Made Easy and Fun, 3rd Edition, Prentice Hall, 2009.
3.	NI Resources: https://learn.ni.com/

COURSE OUTCOMES: **On completion of the course, the students will be able to**		**BT Mapped (Highest Level)**
CO1	describe the components of LabVIEW and virtual instruments	Understanding (K2)
CO2	describe front panel, block diagram and syntax of LabVIEW	Understanding (K2)
CO3	apply the structured programming concepts in developing VI programs	Applying(K3)
CO4	apply the knowledge on DAQ tools for industrial applications	Applying(K3)
CO5	analyze the compact RIO setup for FPGA interfaces.	Analyzing(K4)

Mapping of COs with POs and PSOs

COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1			3	2		
CO2			3	2		
CO3	2	1	3	3		
CO4	2	1	3	3		
CO5	2	2	3	3	1	

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	20	80					100
CAT2	20	40	40				100
CAT3	10	40	50				100
ESE	20	40	40				100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

22ESE10 - WIRELESS SENSOR NETWORKS							
Programme& Branch	**ME &EMBEDDED SYSTEMS**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Computer networks**	**3**	**PE**	**3**	**0**	**0**	**3**
Preamble	To understand and apply the concepts of wireless sensor networks for real world applications.						
Unit – I	**Introduction to Wireless Sensor Networks**						**9**
Introduction – wireless sensor networks (WSNs): Concepts, Components and Architectures, Applications – Network deployment Network Topology –Coverage Metrics-Types of wireless sensor networks.							
Unit – II	**Wireless Personal Area Network:**						**9**
Bluetooth (IEEE 802.15.1)- Bluetooth Protocol Stack- Bluetooth Link Types and security- Network Connection Establishment in Bluetooth- Bluetooth low energy - Zigbee (IEEE 802.15.4)- Zigbee Network Protocol Stack- IEEE 802.15.4 LR-WPAN Device Architecture-Applications.							
Unit – III	**WSN MAC:**						**9**
Physical and Data link layer -Fundamentals of MAC Protocols, MAC Protocols for WSNs- B-MAC, S-MAC-Superframe Structure-Frame formats-CSMA/CA- Case Studies: CSMA, WSN MAC							
Unit – IV	**Mobile Network Layer:**						**9**
Introduction - Mobile IP: IP packet delivery, Agent discovery, tunneling and encapsulation, 6LOWPAN architecture, frame format, Routing Protocol: AODV, LEACH							
Unit – V	**Case Studies and Real-World Applications:**						**9**
Building IOT with RASPERRY PI - Linux on Raspberry Pi – Raspberry Pi Interfaces -Programming Raspberry Pi with Python - Other IoT Platforms – Arduino/ NodeMCU.							
							Total:45

REFERENCES:

1.	Vijay K. Garg, "Wireless Communications and Networking", 1st Edition, Morgan Kaufmann Publishers, USA, 2010
2.	Bhaskar Krishnamachari, “Networking wireless sensors”, Cambridge Press 2005
3.	Zach Shelby, Carsten Bormann, “6LoWPAN The Wireless Embedded Internet”, Wiley 2009

COURSE OUTCOMES: On completion of the course, the students will be able to		BT Mapped (Highest Level)
CO1	interpret various WSN topology and models	Understanding (K2)
CO2	illustrate the functionalities of personal area wireless systems	Understanding (K2)
CO3	choose MAC protocols for wireless sensor networks	Applying(K3)
CO4	apply L2, L3 distinct protocols for WSN environment	Applying(K3)
CO5	deploy IoT applications and analyze in real time scenario	Applying(K3)

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2		3		3	
CO2	2		3			
CO3	3		3	2	2	
CO4	3		3	3	3	
CO5	3	2	3	3	3	2

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1	20	80					100
CAT2	20	45	35				100
CAT3	20	35	45				100
ESE	10	50	40				100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

22ESE11 - PROGRAMMING INTERNET OF THINGS							
Programme& Branch	**ME &EMBEDDED SYSTEMS**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**3**	**PE**	**3**	**0**	**0**	**3**
Preamble	To learn the fundamentals of this emerging technology and to design of smart objects that provide collaboration and ubiquitous services.						
Unit – I	**IoT ARCHITECTURE:**						**9**
IoT Architecture-State of the Art –Reference Model and architecture, IoT reference Model - IoT Reference Architecture, Functional View, Information View, Deployment and Operational View, Other Relevant architectural views. Real-World Design Constraints- Introduction, Technical Design constraints- Data representation and visualization, Interaction and remote control. -IoT Communication Models-Communication API's-IoT Enabling Technologies.							
Unit - II	**IoT LEVELS, M2M, AND SYSTEM MANAGEMENT**:						**9**
IoT Levels1 to 6—M2M-Difference between IoT and M2M –SDN and NFV-Need of IoT system Management- with NETCONF and YANG, IoT Design Methodology.							
Unit - III	I**NTEROPERABILITY IN IoT, INTRODUCTION TO PROGRAMMING PYTHON:**						**9**
Data types – Data structures – Control flow – Functions – Modules – Packages – File Handling – Date and time operation – Classes – Python packages of IoT. IoT Physical Design: Basic building blocks – Raspberry Pi –Linux on Raspberry Pi –GPIO- Interfaces (LED and Switch) – Programming on Raspberry Pi with Python							
Unit - IV	**DATA ANALYTICS AND WEB FRAMEWORK:**						**9**
Data Analytics for IOT: Apache Handoop-Map Reduce Models-Case Study: Batch Data Analysis and Real Time Data Analysis. Web Application Framework: Django, -Django Architecture-starting Development with Django.							
Unit - V	**WEB SERVER INSTALLATIONS AND PROJECT DEVELOPMENT:**						**9**
LAMP Installation– Home temperature monitoring system – Webcam and Raspberry Pi camera project, A Raspberry Pi LASER trip wire, Line follower Robot.							
							Total:45

REFERENCES:

1.	ArshdeepBahga, Vijay K. Madisetti—Internet of Things: A Hands-on Approach, 1stEdition, Universities Press-Hyderabad, 2015.
2.	Donald Norris —The Internet of Things: Do-It-Yourself at Home Projects for Arduino, Raspberry Pi and Beagle Bone Black, 1st Edition, McGraw Hill, 2015
3.	Peter Waher — Learning Internet of Things, 1st Edition, Packt Publishing Limited - USA, 2015.
4.	https:\\projects. Raspberry Pi.org

COURSE OUTCOMES: **On completion of the course, the students will be able to**		**BT Mapped (Highest Level)**
CO1	compare the IoT physical and logical Architecture and its Enabling Technologies	Understanding (K2)
CO2	interpret differentIoT Levels and Networking Methodologies	Understanding (K2)
CO3	implement IoT Programming Concepts using Python and its Open-Source Tools	Applying(K3)
CO4	perform Data Analysis using –Hadoop&, Django	Applying(K3)
CO5	design and integrate projects using Raspberry Pi with Temperature Sensor, Webcam	Applying(K3)

Mapping of COs with POs and PSOs

COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1			2	3		
CO2			2	3		
CO3	2		3	2		
CO4	2		2	3		
CO5	2	2	3	3	3	2

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	20	80					100
CAT2	20	40	40				100
CAT3	10	40	50				100
ESE	20	40	40				100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

22ESE12 - SYSTEM ON CHIP FOR EMBEDDED APPLICATIONS							
Programme& Branch	**ME &EMBEDDED SYSTEMS**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**3**	**PE**	**3**	**0**	**0**	**3**

Preamble	To know the architecture of embedded ARM processor and to study the concepts of operating systems	
Unit – I	**Introduction to System on Chip Design:**	**9**
Processor architecture and organization, Abstraction in hardware design, MU0 - a simple processor, Instruction set design, Processor design trade-offs, The Reduced Instruction Set Computer, Design for low power consumption, ARM architecture.		
Unit – II	**ARM Organization and Implementation:**	**9**
3-stage pipeline ARM organization, 5-stage pipeline ARM organization, ARM instruction execution and implementation, coprocessor interface, The ARM instruction set and programming.		
Unit – III	**ARM Processor Cores and Memory Hierarchy:**	**9**
ARM7TDMI, ARM8, and ARM9TDMI ARM10TDMI - Memory size and speed, On-chip memory, Caches, Cache design - an example, Memory management.		
Unit – IV	**Architectural Support for Operating Systems:**	**9**
An introduction to operating systems, The ARM system control coprocessor,CP15 protection unit registers, ARM protection unit, CP15 MMU registers, ARM MMU architecture, Synchronization, Context switching, Input/output.		
Unit – V	**Embedded ARM Applications:**	**9**
The VLSI Ruby II Advanced Communication Processor, The VLSI ISDN Subscriber Processor, The Ericsson-VLSI Bluetooth Baseband Controller, The ARM7500 and ARM7500FE, case study on The DRACO telecommunications controller		
		Total:45

REFERENCES:

1.	Steve Furber. ARM System-on-Chip Architecture, 2nd Impression, Pearson Education, 2009.
2.	Andrew N. Sloss , DominicSymes, Chris Wright. ARM System Developer's Guide: Designing and Optimizing System Software, 1st Edition, Morgan Kaufmann Publishers, 2004.
3.	Joseph Yiu. The Definitive Guide to ARM® Cortex®-M3 and Cortex®-M4 Processors, 3rd Edition, Newnes publication, 2014.
4.	Yifeng Zhu. Embedded Systems with ARM Cortex-M Microcontrollers in Assembly Language and C, 3rd Edition, E-Man Press LLC, 2017.

COURSE OUTCOMES: On completion of the course, the students will be able to		BT Mapped (Highest Level)
CO1	identify the basic design of system on chip with ARM architecture as a reference	Understanding (K2)
CO2	know the 3-line and 5-line pipelining concept of ARM organization and programming with instruction set	Understanding (K2)
CO3	construct the memory hierarchy and experiment with different ARM7, ARM8, ARM9 and ARM10 processor cores	Applying(K3)
CO4	model the concept of ARM operating systems, ARM protection unit and MMU.	Applying(K3)
CO5	apply the system on chip concept for different embedded applications such as ISDN, Bluetooth and DRACO telecommunication controller	Applying(K3)

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1			3	2		
CO2			3	2		
CO3	2		3	2		
CO4	2		3	2		
CO5	3		3	2		2

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1	30	70					100
CAT2	10	60	30				100
CAT3	10	50	40				100
ESE	10	50	40				100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

22ESE13 - SENSORS AND ENGINE MANAGEMENT SYSTEM							
Programme& Branch	**ME &EMBEDDED SYSTEMS**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**3**	**PE**	**3**	**0**	**0**	**3**

Preamble	To learn the concepts and analyze the uses of sensors in automotive systems and apply the various novel methods to develop electronic based automobile devices for all vehicle conditions.	
Unit – I	**Sensors and Actuators in Automotive Systems:**	**9**
Evolution and Development of electronics in automobiles- Electrical and Electronic Principles – Measurements – Sensors – Thermistors – Thermocouples – Inductive Sensor – Hall Effect – Strain gauge – Variable Capacitive – Variable Resistance – Knock Sensors – LVDT – Hot wire air flow – Thin film air flow – Vortex flow – Pitot tube – Turbine fluid flow sensor – optical sensors – Oxygen sensors – Light sensors – Thick flim air temperature sensor – Methanol – Rain – Oil – Dynamic vehicle position sensor – Actuators – Solenoid Actuators – EGR Valve – Motorized – Stepper motor – Synchronous – Thermal Actuators. Standards and Norms – Euro Norms – Bharat Norms – Emission Testing		
Unit – II	**Batteries, Charging and Starting systems:**	**9**
Vehicle batteries requirements, choosing battery and positioning – Lead acid batteries – Maintenance, charging and testing batteries – Working of charging system – Circuit diagram – Rectification methods – Types of Alternators – Smart Charging. Requirements of starting system – Starter motor and Circuits – DC Characteristics – Types of Starter motors		
Unit – III	**Ignition and Injection Systems:**	**9**
Ignition systems: Ignition fundamentals – Electronic ignition systems – Electronic Spark Ignition advance – Distribution less Ignition – Coil on plug ignition – Spark Plugs. Electronic fuel Control – Basics of combustion – Engine fuelling and exhaust emissions – Electronic control of carburetion – Fuel Injection – Petrol fuel injection – Diesel fuel injection.		
Unit – IV	**Engine Management System:**	**9**
Combined ignition and fuel systems– Exhaust Emission control – Catalytic converter – EGR – SCR – DeNox Trap – Motronic M3 – DI Motronic – ME Motronic principles – Lean burn engine – 2 stroke engine – Combustion control system – Active Cooling - Engine trends – spark ignition – Transonic combustion – Formula 1 engine technology – Diagnosing engine management systems. Case study of Plug-in Hybrid Electric Vehicles (PHEV).		
Unit – V	**Chassis, Comfort and Safety Systems:**	**9**
Antilock braking system – Traction and Stability Control – Active Suspension – Electronic control of automatic transmission – Cruise control – Adaptive cruise control – Security – Airbag and Seat belt tensioners. Centralized door locking system – Climate control of cars – Obstacle avoidance Radar – Automatic Parking System. Electric vehicles – Vehicle Layout – Charging system. In vehicle networks: CAN, LIN, FLEXRAY, MOST, KWP2000		
		Total:45

REFERENCES:

1.	Tom Denton, Automobile Electrical and Electronics Systems, 4th Edition, Edward Arnold Publishers, London, 2013.
2.	Ribbens William B, Understanding Automotive Electronics, 7th Edition, Butterworth- Heinemann, Burlington, 2012.
3.	Tim, Gilles, Automotive Engines: Diagnosis, Repair, Rebuilding, 7th Edition, Delmar Publishers, New York, 2015.
4.	Robert Bosch GmbH, Automotive Hand Book, 9th Edition, Wiley, 2014.

COURSE OUTCOMES: **On completion of the course, the students will be able to**		**BT Mapped (Highest Level)**
CO1	adapt to the continuous changes in emission norms of India and uses of sensors and actuators in automobile applications.	Understanding (K2)
CO2	identify the operations of charging and starting techniques involved in vehicles.	Applying(K3)
CO3	choose appropriate electronic ignition and fuel injection system for automobiles	Applying(K3)
CO4	apply the engine and fuel control system for ECU used in engine management system	Applying(K3)
CO5	employ the essential comfort and safety systems for automobile.	Applying(K3)

Mapping of COs with POs and PSOs

COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	3	1				
CO2	3	2	1	1		
CO3	3	2	1	1		
CO4	3	2	1	1		
CO5	3	2	1	1		

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	20	50	30				100
CAT2	10	40	50				100
CAT3	10	40	50				100
ESE	10	60	30				100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

22ESE14 – NATURE INSPIRED OPTIMIZATION TECHNIQUES							
Programme& Branch	**ME &EMBEDDED SYSTEMS**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**3**	**PE**	**3**	**0**	**0**	**3**

Preamble	To acquaint and familiarize with different types of optimization techniques, solving optimization problems, implementing computational techniques, abstracting mathematical results and proofs etc.	
Unit – I	**Optimization Methods and Algorithms:**	**9**
Newton's Method – Optimization – Search for Optimality – No-Free-Lunch Theorems – 1.6 Nature-Inspired Metaheuristics – Brief History of Metaheuristics. Analysis of Algorithms: Introduction – Analysis of Optimization Algorithms – Nature-Inspired Algorithms – Parameter Tuning and Parameter Control.		
Unit – II	**Simulated Annealing:**	**9**
Annealing and Boltzmann Distribution – Parameters – SA Algorithm – Unconstrained Optimization – Basic Convergence Properties – SA Behavior in Practice – Stochastic Tunneling. Genetic Algorithms: Introduction – Genetic Algorithms – Role of Genetic Operators – Choice of Parameters - GA Variants – Schema Theorem – Convergence Analysis		
Unit – III	**Particle Swarm Optimization:**	**9**
Swarm Intelligence – PSO Algorithm – Accelerated PSO – Implementation – Convergence Analysis – Binary PSO – Problems. Cat Swarm Optimization: Natural Process of the Cat Swarm – Optimization Algorithm – Flowchart – Performance of the CSO Algorithm.		
Unit – IV	**TLBO Algorithm, Cuckoo Search & Bat Algorithms:**	**9**
TLBO Algorithm: Introduction – Mapping a Classroom into the Teaching-Learning- Based optimization – Flowchart-Problems. Cuckoo Search: Cuckoo Life Style – Details of COA – flowchart –Cuckoos' Initial Residence Locations – Cuckoos' Egg Laying Approach – Cuckoos Immigration –Capabilities of COA. Bat Algorithms – Echolocation of Bats – Bat Algorithms – Implementation – Binary Bat Algorithms – Variants of the Bat Algorithm – Convergence Analysis		
Unit – V	**Hybrid algorithms for optimization:**	**9**
Ant Algorithms – Bee-Inspired Algorithms – Harmony Search – Hybrid Algorithms		
		Total:45

REFERENCES:

1.	Xin-She Yang, Nature-Inspired Optimization Algorithms, 1st Edition, Elsevier, 2014
2.	OmidBozorg-Haddad, Advanced Optimization by Nature-Inspired Algorithms Studies in Computational Intelligence,1st Edition, Springer Series, 2018
3.	Srikanta Patnaik, Xin-She Yang,Kazumi Nakamatsu, Nature-Inspired Computing and Optimization Theory and Applications, 1st Edition, Springer Series, 2017

COURSE OUTCOMES: **On completion of the course, the students will be able to**		**BT Mapped (Highest Level)**
CO1	infer the concepts of optimization techniques	Understanding (K2)
CO2	identify the parameter which is to be optimized for an application	Applying(K3)
CO3	differentiate the concepts of different optimization algorithms and create mathematical optimization models	Applying(K3)
CO4	select suitable optimization algorithm for a real time application	Applying(K3)
CO5	make recommendations to solve combinatorial optimization problems	Applying(K3)

Mapping of COs with POs and PSOs

COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	2		3	2		
CO2	1		2	3		
CO3	2		3	2		
CO4	3		2	3		2
CO5	2		2	3		2

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN – THEORY

Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	10	50	40				100
CAT2	10	50	40				100
CAT3	10	50	40				100
ESE	10	50	40				100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

22VLE17- SUPERVISED MACHINE LEARNING ALGORITHMS (Common to VLSI Design and Embedded Systems branches)							
Programme& Branch	**ME - VLSI DESIGN & ME - EMBEDDED SYSTEMS**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**3**	**PE**	**3**	**0**	**0**	**3**
Preamble	To focus on supervised machine learning algorithms and to create simple, interpretable models to solve classification and regression problem						
Unit – I	**Discriminative Algorithms :**						**9**
Cost function –LMS Algorithm – The normal Equations-Probability interpretation-locally weighted linear regression-logistic regression- generalized linear models-Application to prediction.							
Unit – II	**Generative Algorithms :**						**9**
Generative Models: Gaussian Discriminant Analysis (GDA)-Naïve Bayes- Laplace smoothing-Marginal classifier: Support Vector Machine (SVM) as optimal Margin classifier-Application to Classification.							
Unit – III	**Multilayer Perceptrons:**						**9**
Multilayer Perceptrons-Implementation of Multilayer Perceptrons-Forward Propagation, Backward Propagation and computer Graphs-Numerical stability and Initialization-Generalization in Deep Learning-Dropout-Case study: House Price Prediction.							
Unit – IV	**Convolutional Neural Networks (CNN) :**						**9**
From fully Connected Layers to Convolutions –Convolution for Images-Padding and Stride-Multiple input and multiple output channel-Pooling-Case study: LeNet, Alexnet, VGGnet.							
Unit – V	**Recurrent Neural Network(RNN):**						**9**
Working with sequences-Converting Raw Text into Sequence Data-Language model-Recurrent Neural Network-Back Propagation through time-Case study: GRU,LSTM.							
							Total:45

REFERENCES:

1.	Christopher M. Bishop, “Pattern Recognition and Machine Learning”, Springer-Verlag New York. reprint 2010
2.	Aston Zhang, Zachary C. Lipton, Mu Li, and Alexander J. Smola,”Dive into Deep learning”, ebook Published September 18, 2020 https://d2l.ai/index.html
4.	UCI Machine Learning repository: http://archive.ics.uci.edu/ml/index.php

COURSE OUTCOMES: **On completion of the course, the students will be able to**		**BT Mapped (Highest Level)**
CO1	understand discriminative algorithms for classification and regression problems	Understanding(K2)
CO2	validate a generative model based algorithm for classification and regression problems	Applying (K3)
CO3	understand the designed ANN for a real time application using BPN	Understanding(K2)
CO4	develop a CNN model for image analysis	Applying(K3)
CO5	develop a RNN model for various types of sequence	Applying (K3)

Mapping of COs with POs and PSOs

COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	3				3	3
CO2	3		3		3	3
CO3	3		3		3	3
CO4	3		3		3	3
CO5	3		3		3	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN – THEORY

Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	10	50	40	-	-	-	100
CAT2	10	50	40	-	-	-	100
CAT3	10	50	40				100
ESE	5	45	50	-	-	-	100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

22ESE03 - DESIGN OF EMBEDDED SYSTEMS							
Programme& Branch	**ME &EMBEDDED SYSTEMS**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**3**	**PE**	**3**	**0**	**0**	**3**

Preamble	To understand the design and use of single-purpose processors, general-purpose processors and to describe memories and buses.	
Unit – I	**Embedded Design Life Cycle:**	**9**
Embedded Design life cycle – Product specification – Hardware / Software partitioning –Detailed hardware and software design – Integration – Product testing Selection Processes – Microprocessor Vs Micro Controller – Performance tools – Bench marking – RTOS availability – Tool chain availability – Other issues in selection processes.		
Unit – II	**Partitioning Decision:**	**9**
Hardware / Software duality – Coding Hardware – ASIC revolution - Managing the Risk – Co-verification – Execution environment – Memory organization –System startup – Hardware manipulation – Memory mapped access –Speed and code density.		
Unit – III	**Emulator:**	**9**
Interrupt Service routines – Watch dog timers – Flash memory Basic toolset – Host Based debugging – Remote debugging – ROM emulators – logic Analyzer – Caches – Computer optimization – Statistical profiling.		
Unit – IV	**In-Circuit Emulators:**	**9**
Bullet proof run control – Real time trace – Hardware break points – Overlay memory – Timing constraints – Usage issues – Triggers.		
Unit – V	**Testing:**	**9**
Bug tracking – reduction of risks & costs – Performance – Unit testing – Regression testing – Choosing test cases – Functional tests – Coverage tests – Testing embedded software – Performance testing – Maintenance		
		Total:45

REFERENCES:

1.	Arnold S. Berger. Embedded System Design, 1st Edition, Taylor& Francis Group, USA 2017.
2.	SriramIyer. Embedded Real time System Programming, Tata McGraw-Hill, India, 2017.
3.	Ronald C Arkin. Behaviour-based Robotics, The MIT Press, 2000.

COURSE OUTCOMES: **On completion of the course, the students will be able to**		**BT Mapped (Highest Level)**
CO1	realize the design flow of an embedded system	Understanding (K2)
CO2	comprehend partitioning decision involved in embedded system design	Understanding (K2)
CO3	utilize basic tool set used for debugging software and hardware	Applying (K3)
CO4	use various in- circuit tool sets for debugging embedded hardware and memories	Applying(K3)
CO5	apply different testing methods involved in test phase for the design of embedded system	Applying(K3)

Mapping of COs with POs and PSOs

COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	2		3	2	2	
CO2			2	3	1	
CO3	2		2	3		
CO4	2		2	3		2
CO5	2		2	3		3

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	10	90					100
CAT2	10	50	40				100
CAT3	-	55	45				100
ESE	10	45	45				100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

22GET13 - INNOVATION, ENTREPRENEURSHIP AND VENTURE DEVELOPMENT							
(Common to ME/MTech and MCA Programmes)							
Programme & Branch	**All ME/MTech and MCA Programmes**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**3**	**PE**	**3**	**0**	**0**	**3**
Preamble	This course will direct the students on how to employ their innovations towards a successful entrepreneurial venture development.						
Unit – I	**Innovation and Entrepreneurship:**						**9**
Creativity and Innovation – Types of innovation – challenges in innovation- steps in innovation management- Meaning and concept of entrepreneurship - Role of Entrepreneurship in Economic Development - Factors affecting Entrepreneurship – Entrepreneurship vs Intrapreneurship.							
Unit – II	**Design Thinking and Product Design:**						**9**
Design Thinking and Entrepreneurship – Design Thinking Stages: Empathize – Define – Ideate – Prototype – Test. Design thinking tools: Analogies – Brainstorming – Mind mapping. Techniques and tools for concept generation, concept evaluation – Product architecture –Minimum Viable Product (MVP)- Product prototyping – tools and techniques– overview of processes and materials – evaluation tools and techniques for user-product interaction.							
Unit – III	**Business Model Canvas (BMC) and Business Plan Preparation:**						**9**
Lean Canvas and BMC - difference and building blocks- BMC: Patterns – Design – Strategy – Process–Business model failures: Reasons and remedies. Objectives of a Business Plan - Business Planning Process and Preparation.							
Unit – IV	**IPR and Commercialization:**						**9**
Need for Intellectual Property- Basic concepts - Different Types of IPs: Copy Rights, Trademarks, Patents, Geographical Indications, Trade Secrets and Industrial Design– Patent Licensing - Technology Commercialization – Innovation Marketing.							
Unit – V	**Venture Planning and Means of Finance:**						**9**
Startup Stages - Forms of Business Ownership - Sources of Finance – Idea Grant – Seed Fund – Angel & Venture Fund – Institutional Support to Entrepreneurs – Bank and Institutional Finance to Entrepreneurs.							
							Total:45

REFERENCES:

1.	Gordon E. & Natarajan K., "Entrepreneurship Development", 6th Edition, Himalaya Publishing House, Mumbai, 2017.
2.	Sangeeta Sharma, "Entrepreneurship Development", 1st Edition, PHI Learning Pvt. Ltd., New Delhi, 2017.
3.	Charantimath Poornima M., "Entrepreneurship Development and Small Business Enterprises", 3rd Edition, Pearson Education, Noida, 2018.
4.	Robert D. Hisrich, Michael P. Peters & Dean A. Shepherd, "Entrepreneurship", 10th Edition, McGraw Hill, Noida, 2018.

COURSE OUTCOMES: On completion of the course, the students will be able to		BT Mapped (Highest Level)
CO1	understand the relationship between innovation and entrepreneurship	Understanding (K2)
CO2	understand and employ design thinking process during product design and development	Analyzing (K4)
CO3	develop suitable business models as per the requirement of the customers	Analyzing (K4)
CO4	practice the procedures for protection of their ideas IPR	Applying (K3)
CO5	understand and plan for suitable type of venture and modes of finances	Applying (K3)

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	2	1				3	2	1	3	2		1	1	
CO2	1	2			3	2	1						1	
CO3	3	1	3			1							1	
CO4	1	2				3							1	
CO5	1	2				3							1	

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN – THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1	40	40	20				100
CAT2	30	40	30				100
CAT3	30	40	30				100
ESE	30	40	30				100

* ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)